OPS *net* :

An all-Optical Packet Switched network

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Overview

- Introduction
- Project goals
- Node architecture and design
- Simulations

Introduction

- The **OPS***net* project
  - Researches **optical packet switching**, building upon the results from the earlier **EPSRC** project **WASPNET**
  - Is a collaboration between 3 academic partners:
    - University of Essex
    - University of Cambridge
    - University of Strathclyde
  - Is supported by a number of industrial partners:
    - BT Laboratories, Corning, Fujitsu Telecommunications, Agilent and Marconi Communications

Introduction

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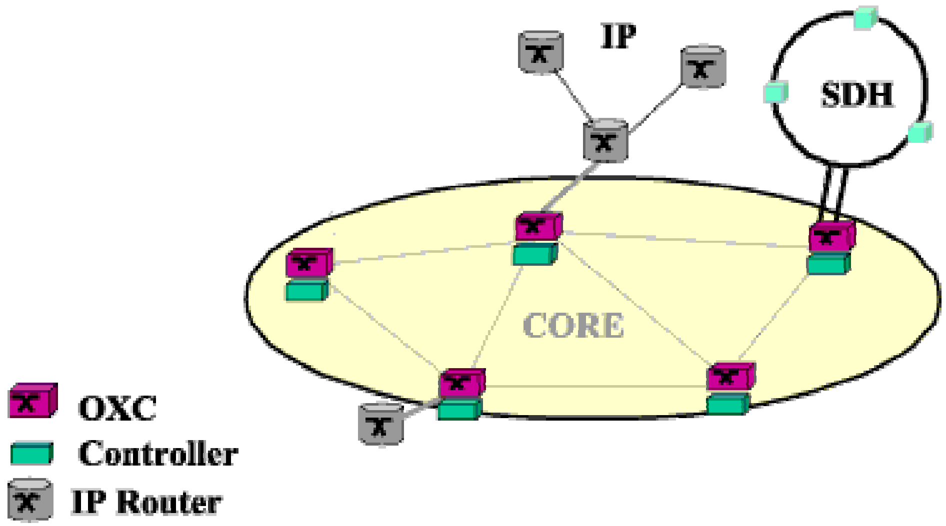
- Today: OXC-based network
  - Main focus of today's optical network R&D: implementing a dynamically reconfigurable optical transport layer based on fast optical cross-connects.
  - Optical transport network will be capable of supporting large numbers of high capacity circuit-switched channels, with bit rates of 10-40 Gb/s.



Introduction

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- In near future: OPS added to the OXC network
  - Optical packet switching (OPS) allows to use bandwidth efficiently and to support diverse services.
  - OPS can appear as a natural evolution of the optical transport network. Designated wavelengths supporting optical packets can be processed within the OPS, other channels can be purely circuit-switched.
  - Maximises utilisation of the optical channels
  - Facilitates restoration and protection

Introduction

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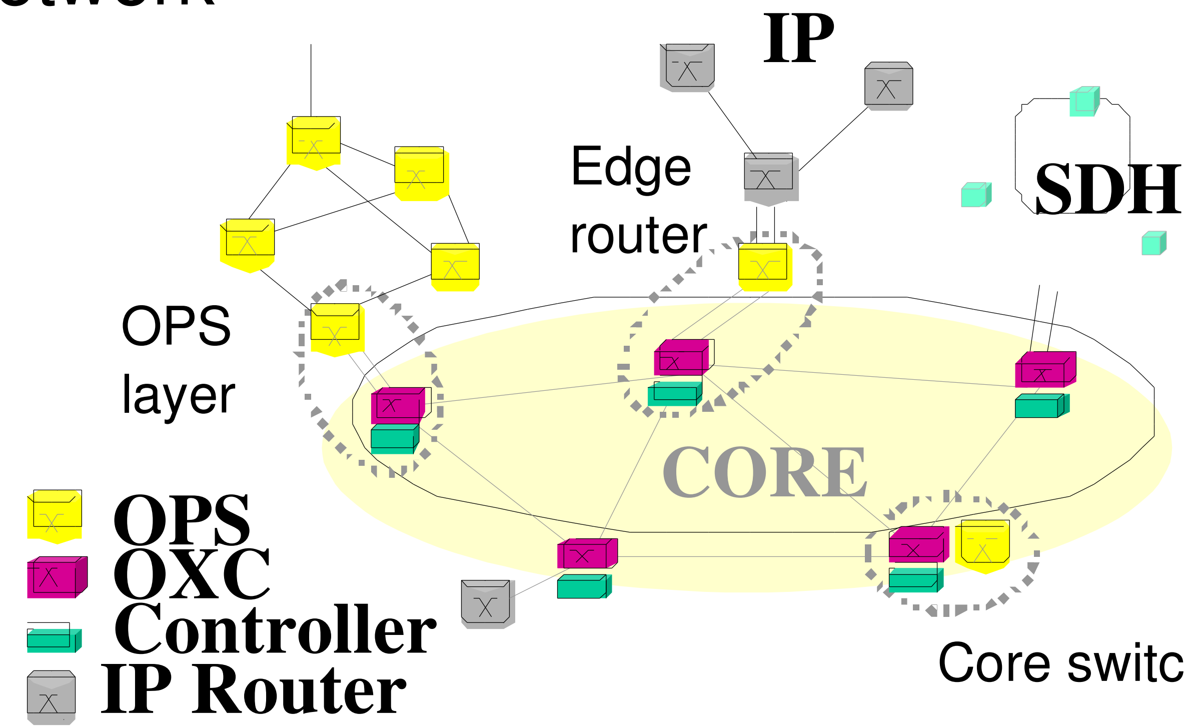
- Possible applications of OPS in a OXC network



OPS*net* Project Objectives

- To **evaluate** the relative performance (and cost) **merits** of synchronous and asynchronous switch and network design for variable length packet transport.
- To **design** and **build** an asynchronous optical packet switch to support variable length packets for 40 Gb/s (with technology scalable to 100 Gb/s).
- To **study** the impact of digital data **traffic** statistics on the asynchronous node design.
- To **demonstrate** an end-to end network path across the IP and optical domains using asynchronous optical packet switching.

WASPNET Switch

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- Key features
  - Synchronous, fixed-length packet switch
  - Contention resolution and prioritisation through buffering
  - Based on wavelength-routing technology (AWG-TWC)
  - Can handle circuit-switched paths

WASPNET Switch Architecture

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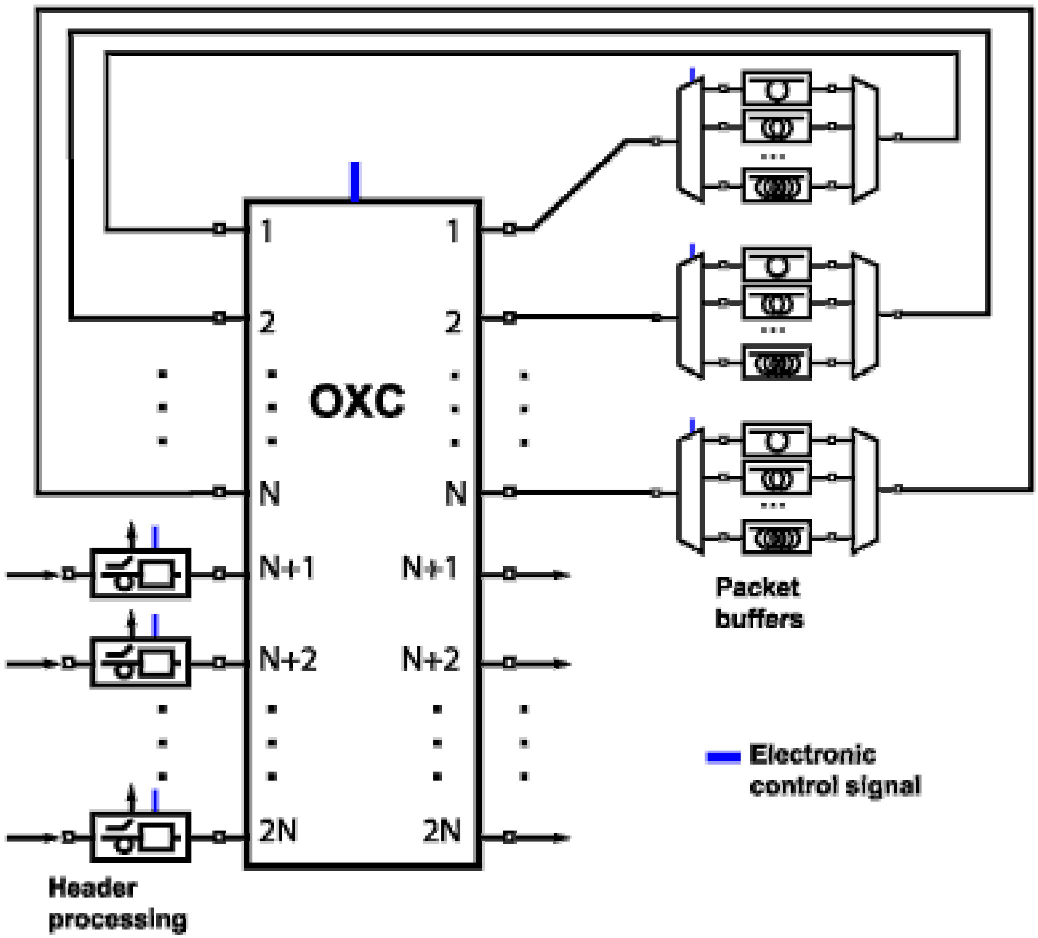
- Node architecture



Key Components

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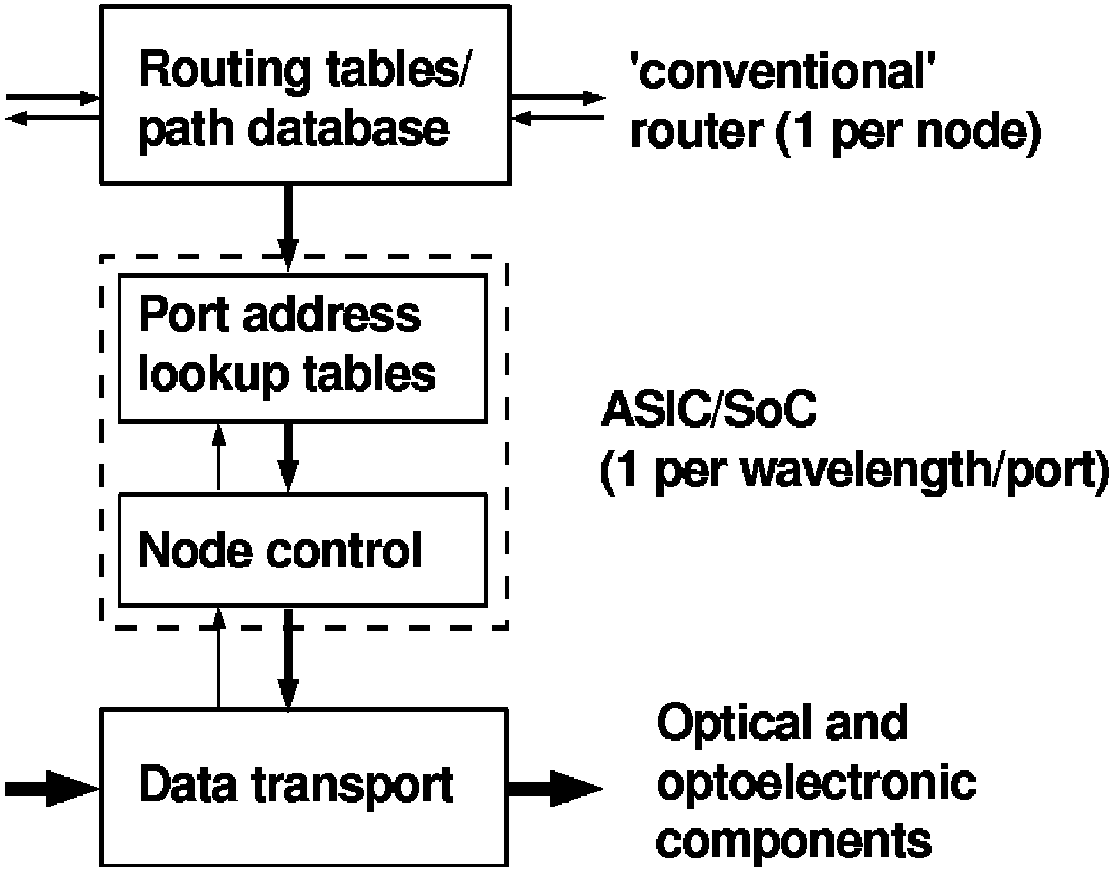
- Fast switches
  - Wavelength switching: tuneable wavelength converter (TWC)
  - Space switching: combine TWC with wavelength router, e.g. AWG.
- Optical amplifiers
  - For recirculating optical buffers: 2R
  - For switching fabric: TWC provides amplification

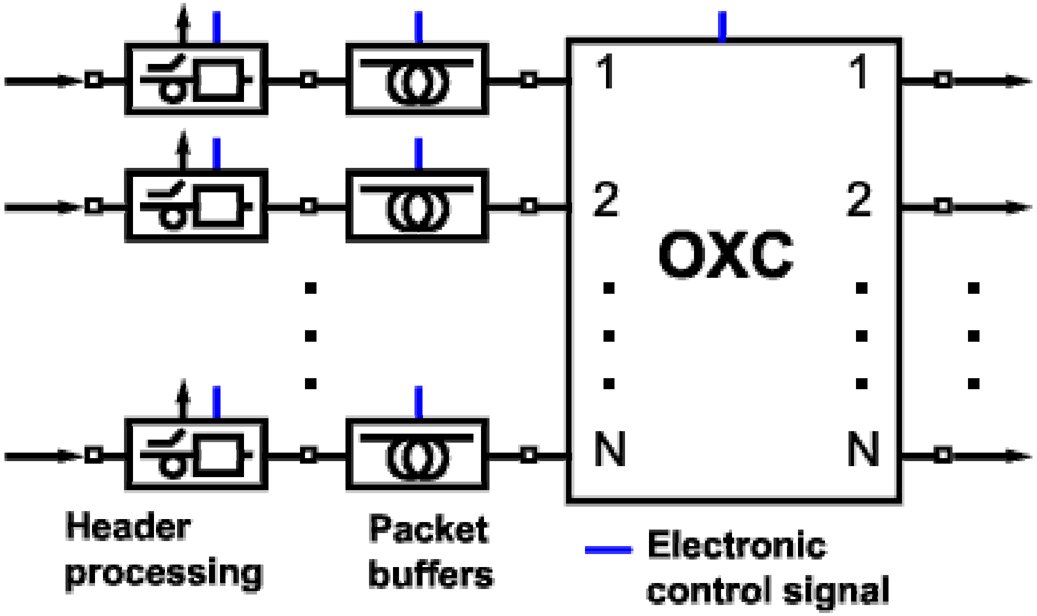
- Key features
  - Asynchronous switching, packets with variable length
  - Prioritisation and contention resolution by buffering
  - Can handle circuit switching
  - DWDM-capable with wavelength translation
  - Scalable

Node Model


Routing tables/
path database
'conventional'
router (1 per node)
Port address
lookup tables
ASIC/SoC
(1 per wavelength/port)
Node control
Data transport
Optical and
optoelectronic
components

OPS with In-line Buffers

- Node architecture



Buffer Design

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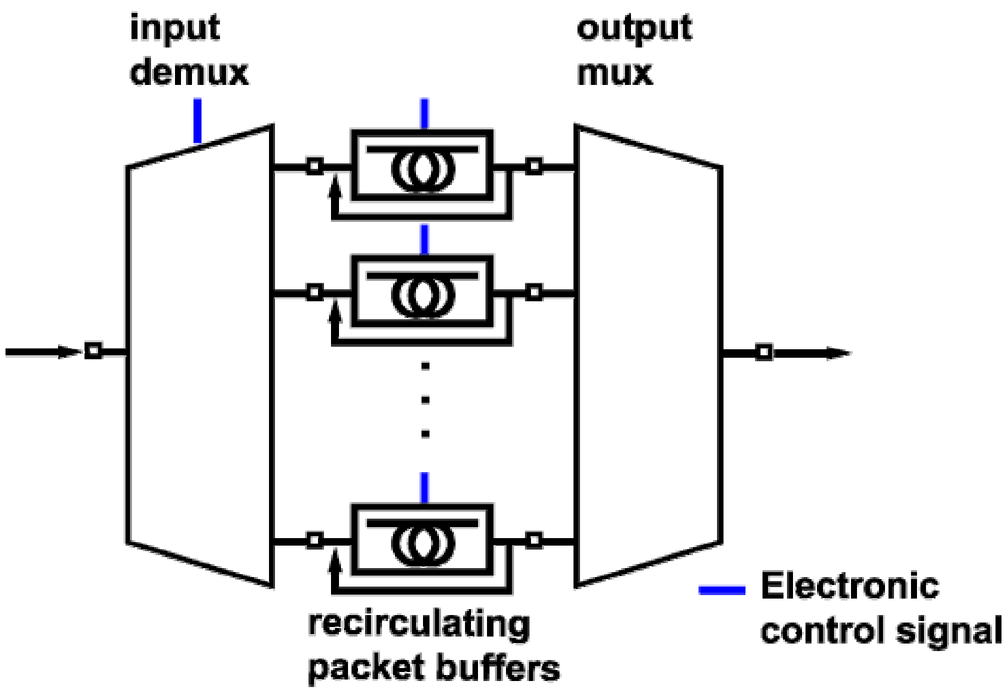
- Parallel recirculating buffers



Buffer Control

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- Event-driven buffer control
  - For every arriving packet:
    - checks for the first free buffer
    - If none, drops the packet
    - Otherwise, stores packet information (length, priority, destination)
  - At every potential exit for any packet, checks:
    - Packet order
    - Packet priority
    - Output port state
  - For every leaving packet:
    - updates the free buffer count and packet order count.
    - Clears the packet information
    - Signals the state of the destination port to other buffer control modules

Node Control Architecture

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- ASIC for speed
  - embedded SRAM
  - one chip per OPS port
- Fast output-port address lookup
  - on-the-fly serial to parallel conversion
  - packet label is SRAM address
  - SRAM contains destination port address and priority (traffic class)
- Asynchronous logic
  - Error checking on header bits
  - Address/Priority lookup
  - Contention detection
  - Buffer control

Functional Modelling

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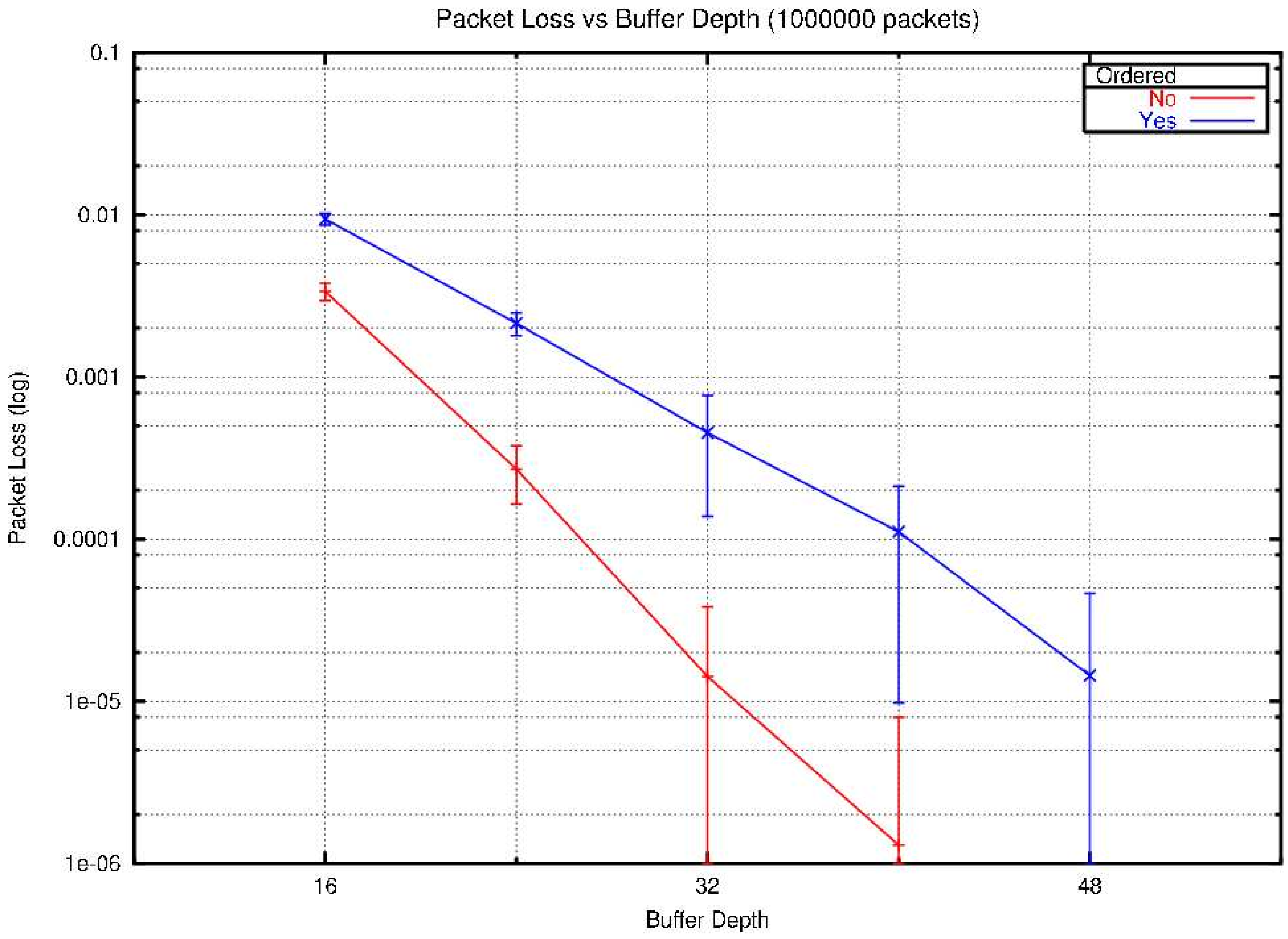
- Functional modelling of opto-electronic systems
  - Abstraction level: functional behaviour of devices/systems
  - Bit-level, digital modelling
- Opto-electronic co-design using HDL
  - Verilog: standardised (IEEE 1364-2001) Hardware Description Language
  - Co-simulation of optical and electronic blocks
  - Simulation at different levels

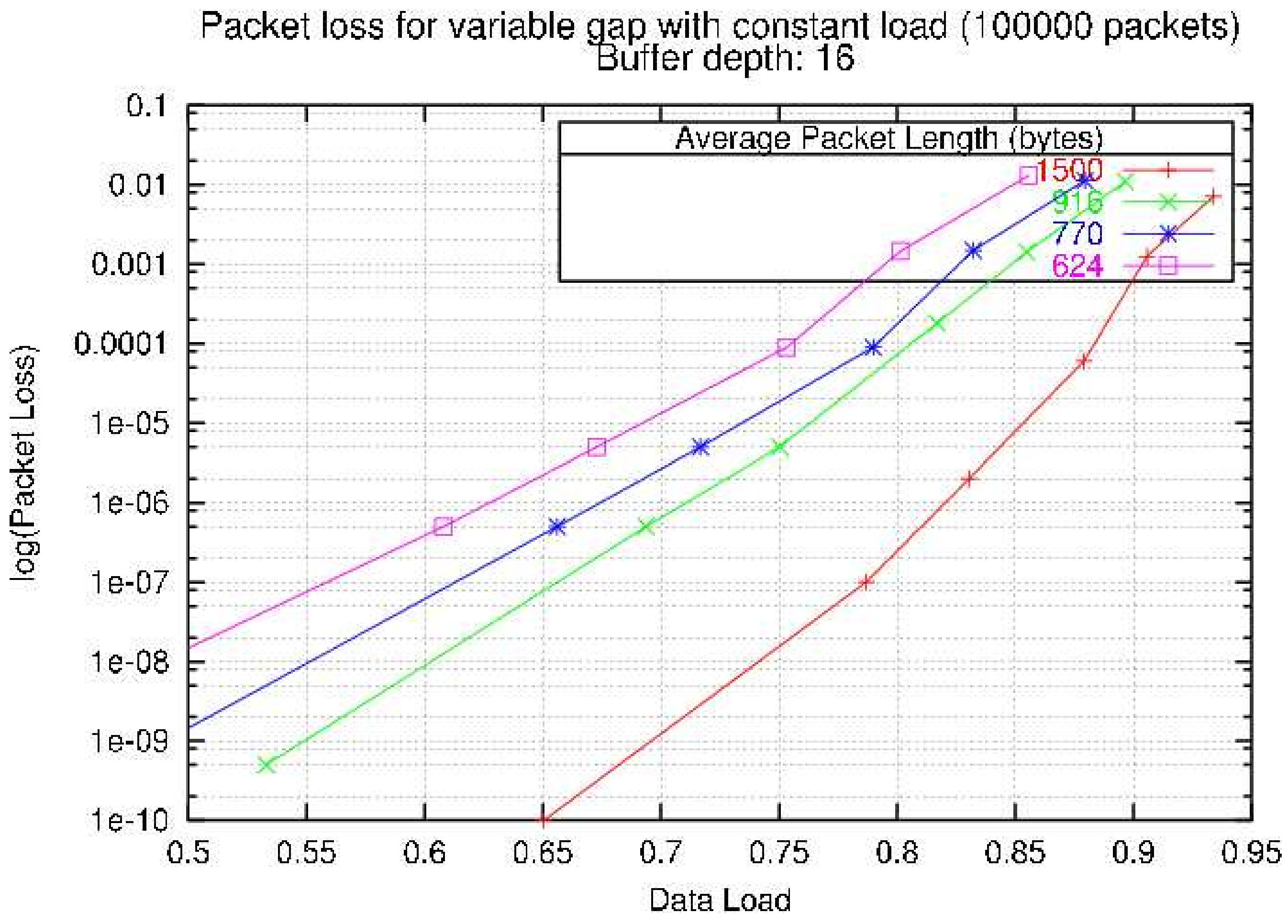
High-level OPS Node Model

- Abstraction of HDL description (node simulator)
  - Port of Verilog model to C++
  - Main purpose:
    - dimensioning of buffer depth and evaluating merits of different buffer designs
    - Study of traffic aggregation at entry points
  - Packet-level simulations
  - Extendable to full network simulations

Buffer Depth Dimensioning



Influence of Network Load



Traffic Shaping

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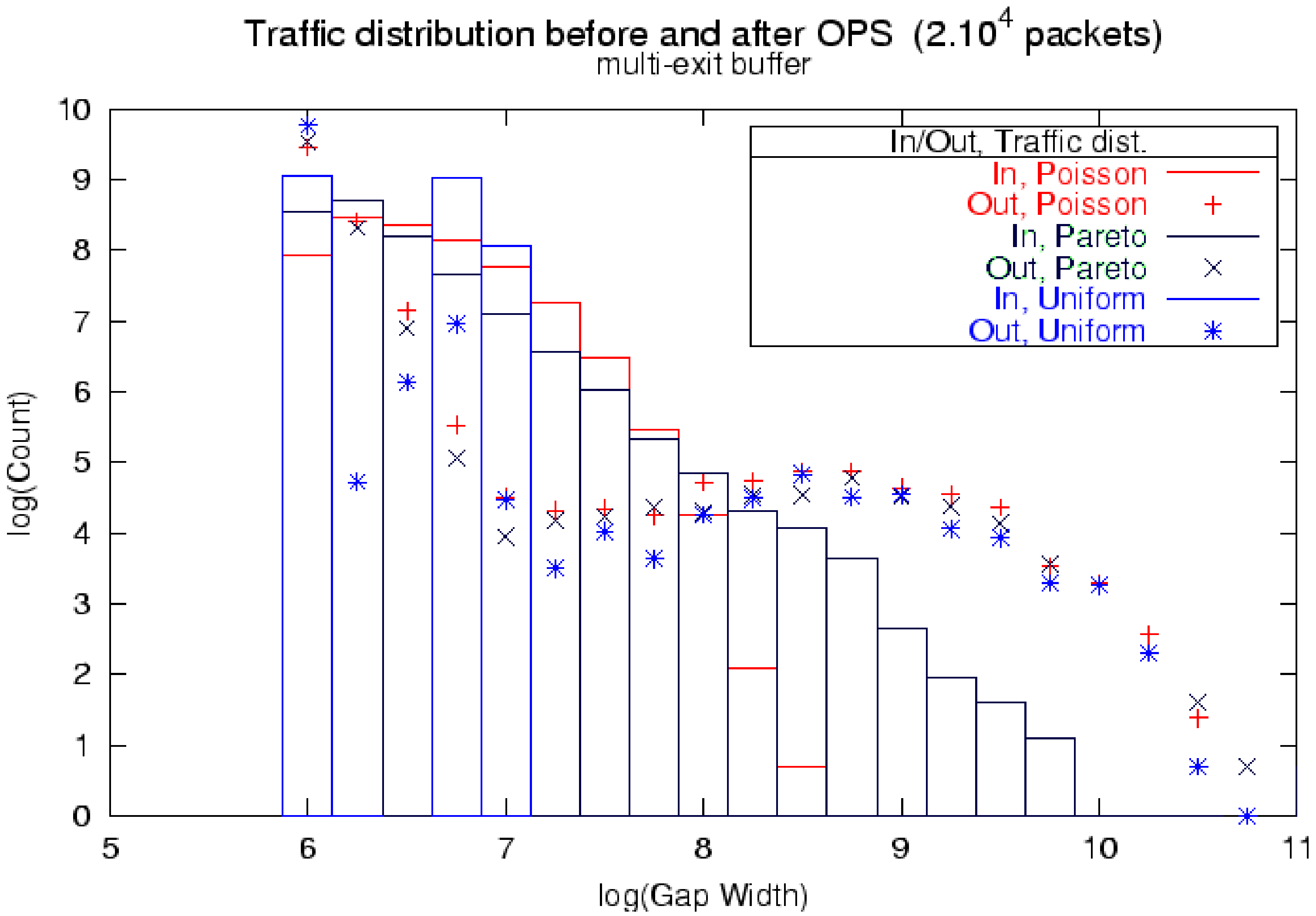
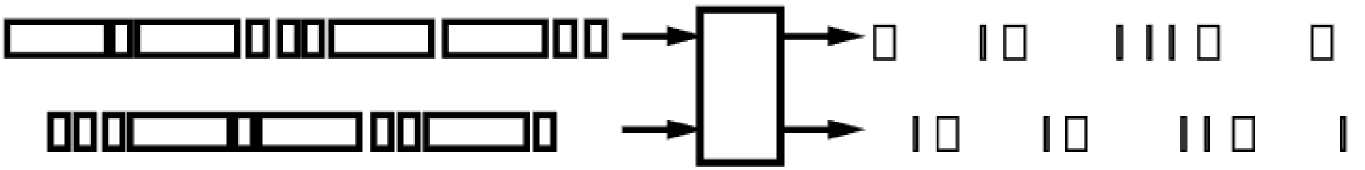


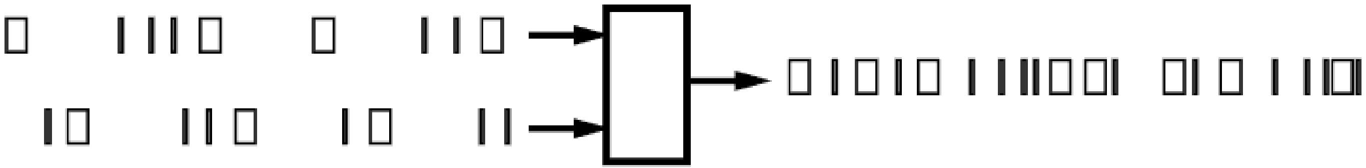
Traffic Aggregator

- Two-stage aggregator

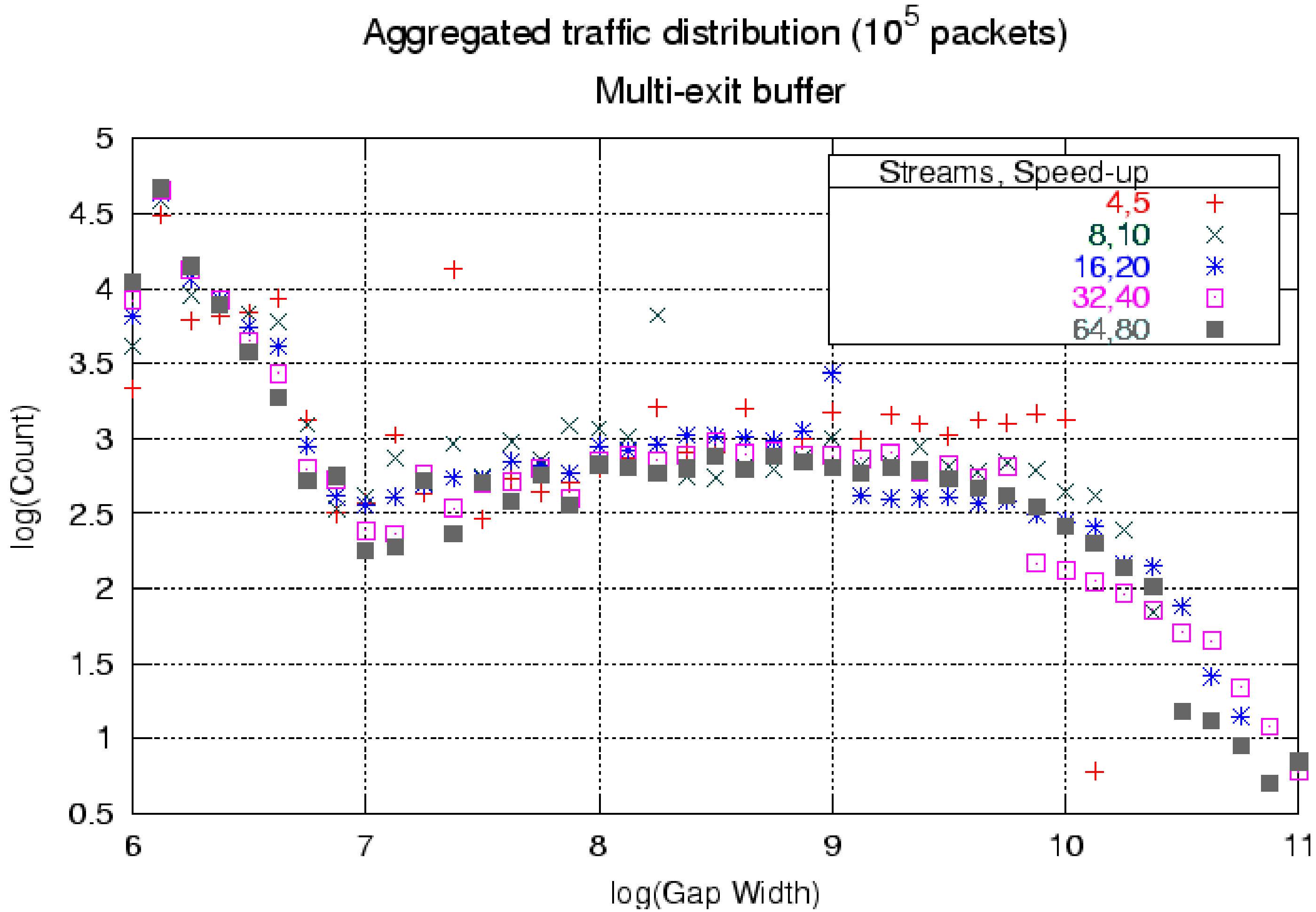
Receive packets at feeder network bitrate
Retransmit at core network bitrate



Aggregate retransmitted packet streams
Traffic aggregator is an OPS with a single output port



Traffic Aggregation



Simulation Results

- Required buffer depth for a given packet loss
  - Depends on gap-width distribution
  - Does not depend strongly on packet length distribution
- OPS with statistical multiplexing shapes traffic
  - Traffic distribution after OPS has only weak correlation to traffic distribution before OPS
  - Characteristics of resulting distribution ensures low packet loss
- OPS used as traffic aggregator
  - Distribution of aggregated traffic is determined by buffer design and packet length distribution
  - Influence of number of streams to be aggregated is small

Conclusion

- We present a new type of OPS
  - Asynchronous switching
  - Packets of variable length
  - In-line parallel recirculating buffer for maximum throughput
  - High load with low packet loss can be achieved
  - OPS can be used as traffic aggregator

GMPLS-compliant Architecture

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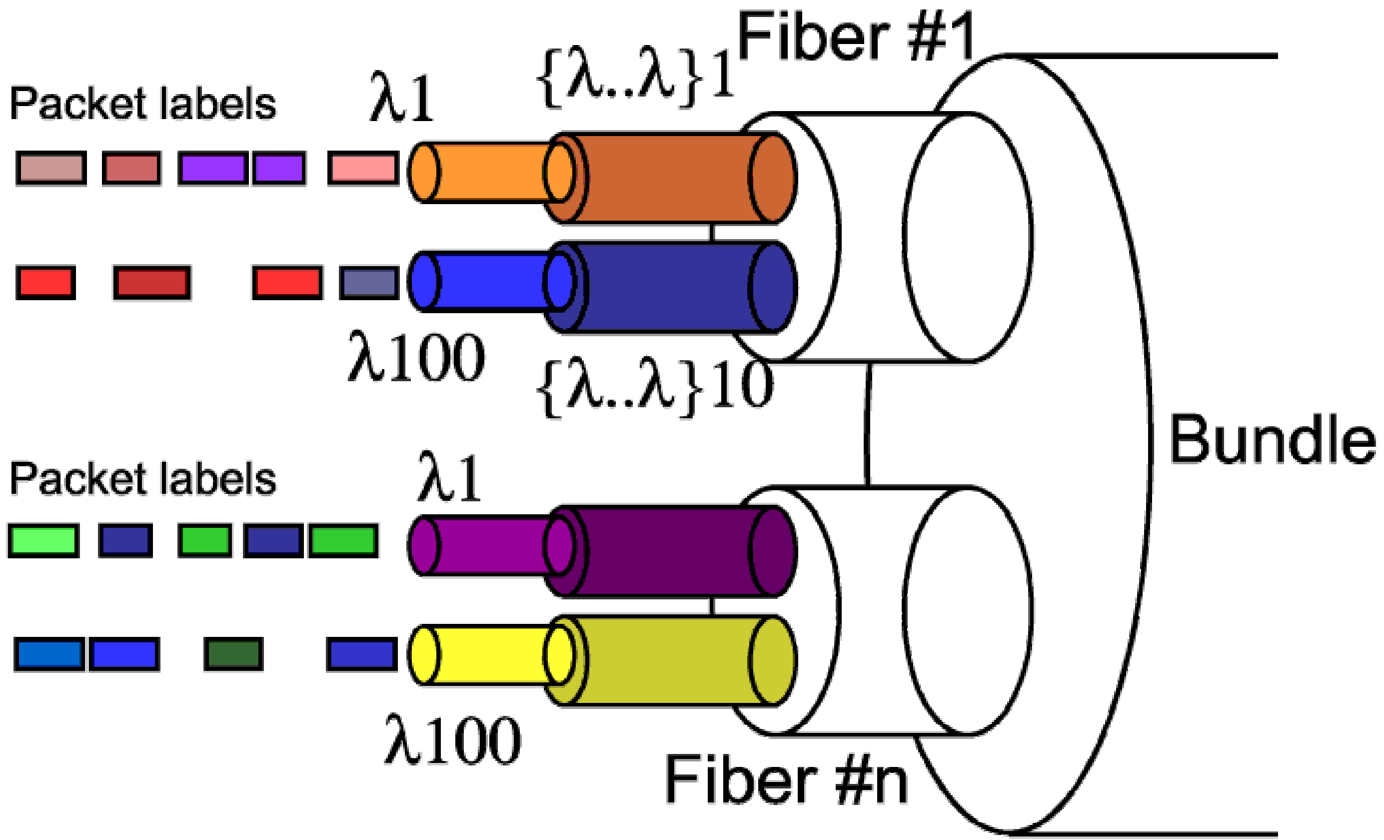
- Support paths with lambda labels, i.e. circuit switching, and packet labels, i.e. optical packet switching.
- Packet labels can be stacked on top of lambda labels (multiplexing)



Project Objectives (1)

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- To evaluate the relative performance (and cost) merits of synchronous and asynchronous switch and network design for variable length packet transport.
  - WASPNET demonstrated a prototype switch within a network environment. OPSnet builds on these results.
  - The WASPNET switch was essentially a synchronous, single-wavelength design. The OPSnet switch will be an asynchronous DWDM OPS with wavelength translation.
- To design and build an asynchronous optical packet switch to support variable length packets for 40 Gb/s (with technology scalable to 100 Gb/s).
  - Due to its synchronous nature, the WASPNET switch worked with fixed packet lengths.
  - The OPSnet switch will allow variable packet lengths, although in a limited range.

Project Objectives (2)

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- To study the impact of digital data traffic statistics on the asynchronous node design.
  - In principle, the network could carry IP packets directly without any intermediate layer.
  - However, for OPSnet an optical packet structure will be proposed; the aggregation of traffic into these packets, the length and spacing of the packets will influence the switch behaviour.
- To demonstrate an end-to end network path across the IP and optical domains using asynchronous optical packet switching.

Architecture and Design Choices

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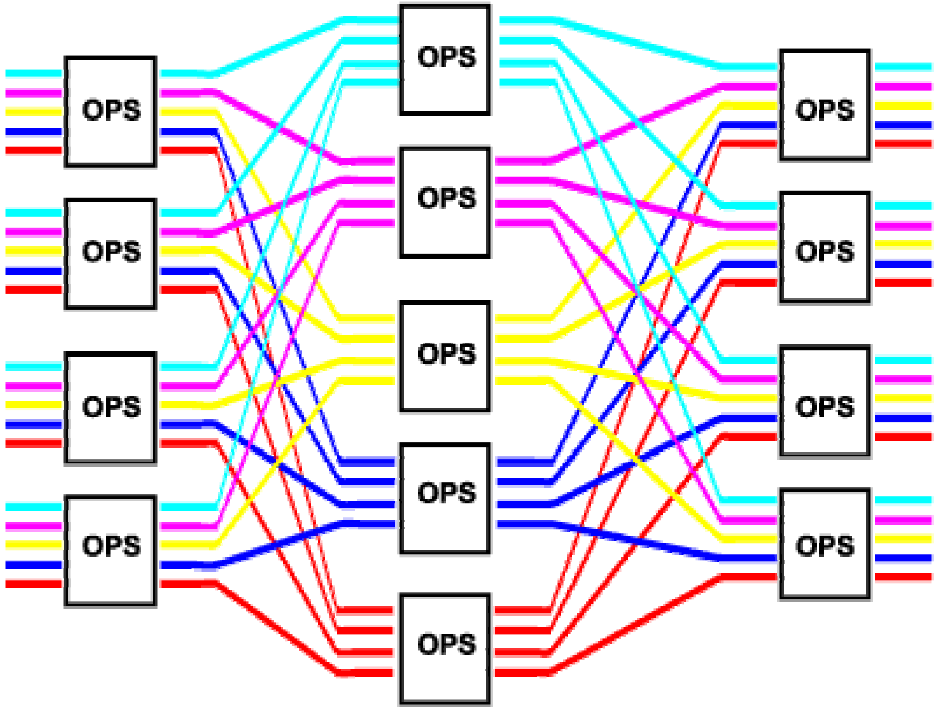
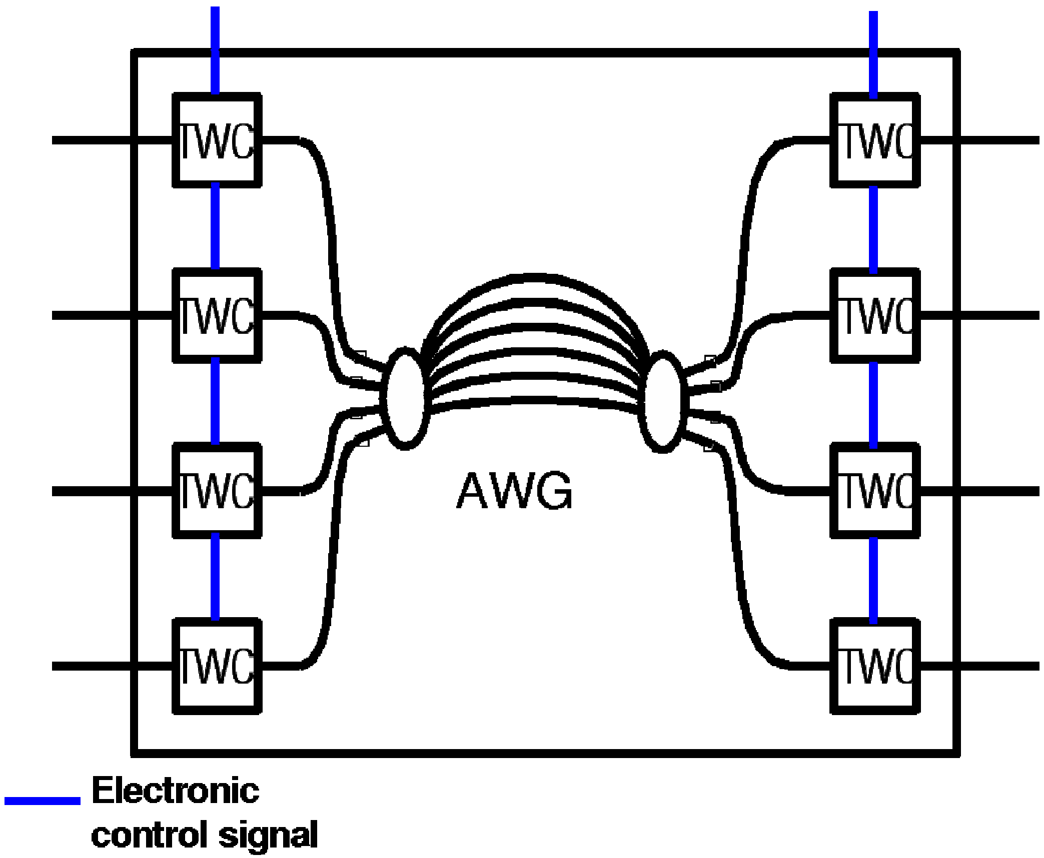
- GMPLS-compliant architecture
  - Support paths with lambda labels, i.e. circuit switching
  - Support packet labels, i.e. optical packet switching
  - Packet labels can be stacked on top of lambda labels (multiplexing)
  - Support for multiple service classes
- Design choices
  - Asynchronous switching
  - Packets with variable length
  - Prioritisation and contention resolution by buffering
  - Fixed header

WDM OPS

- Modular WDM OPS architecture



Space Switch Architecture



Buffer Design Concepts

- One buffer per OPS input port
  - In-line buffer, the packets are buffered by default
  - Parallel per-packet recirculating buffers
  - Multi-exit buffer to increase egress probability
- Egress governed by cascaded conditions
  - Lower-priority packets stay longer in the buffer
  - Packet order for packets to common destination can be conserved
  - In case of buffer overflow, best-effort traffic class packets can be dropped in favour of low-loss class packets