

Dejice Jacob

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Education

PhD, University of Glasgow February 2016 - November 2020

EPSRC funded research titled ‘Opportunistic Acceleration of Array-centric Python Computation in Heterogeneous Environments’ – (doi: [10.5525/gla.thesis.82011](https://doi.org/10.5525/gla.thesis.82011)) under the supervision of Dr. Jeremy Singer and Professor Phil Trinder, School of Computing Science, University of Glasgow. This research was done to further the goals of the EPSRC “AnyScale Apps” project (EP/L000725/1). The work done for the PhD thesis led to three publications [P_9 , P_{11} and P_{12}]. The thesis was shortlisted as one of four finalists for the *SICSA PhD Award for Best Dissertation in Scotland*, 2021.

MSc (Distinction), System Level Integration, iSLI, University of Edinburgh October 2006 - October 2007

Taught modules included VLSI, embedded systems and DSP. My project titled “Software-Centric Design of a Network Co-processor for Embedded systems” was an industrial project developed at Critical Blue, Edinburgh.

BE, Electrical & Electronics Engineering, Regional Engineering College, Trichy, India September 1999 - May 2003

Taught modules included embedded software, digital logic, computer architecture, electrical machines and power distribution. Final year project was the design of an active power filter to dynamically calculate and cancel impedance caused by harmonics. CGPA–7.1/10.

Skills

- Excellent C, C++, Python, Rust and assembler (ARM, RISC-V, x86-64)
- Excellent knowledge of GPU programming in OpenCL (C-dialect) and CUDA
- In-depth knowledge of compiler stacks, Virtual Machine internals, JIT compilers and Garbage Collectors
- Systems level programming knowledge of capability based CHERI architectures
- Software deployment technologies such as Ansible and Docker
- Excellent understanding of Recovery bootloaders and secure firmware update mechanisms for embedded systems
- Very good Low Level device driver and Board Support Package (BSP) development skills for peripherals such as I2C, SPI, HDMI, 802.3 ethernet.

Publications, Prizes and Patent

h-index:6

- P_1 Hunting Wang, Dejice Jacob, David Kelly Jeremy Singer, Yehia Elkhatib and Zheng Wang, 2025 “SecureMind: A Framework for Benchmarking Large Language Models in Memory Bug Detection and Repair” To appear in Proceedings of the 25th International Symposium on Memory Management (ISMM’25) June 16–17, 2025, Seoul, South Korea.
- P_2 Duncan Lowther, Dejice Jacob, Jacob Trevor and Jeremy Singer. 2025 “Secure Scripting with CHERI IoT MicroPython” In Proceedings of the 34th ACM SIGPLAN International Conference on Compiler Construction (CC’25) March 1–2, 2025, Las Vegas, USA. – doi: [10.1145/3708493.3712694](https://doi.org/10.1145/3708493.3712694).
- P_3 Duncan Lowther, Dejice Jacob and Jeremy Singer. 2024 Honourable mention at “[Digital Security by Design Ecosystem Beacon Awards](#)” awarded by FreeBSD foundation for [Capability Boehm](#) and [Morello MicroPython](#). March 21, 2024, Manchester, UK.
- P_4 Duncan Lowther, Dejice Jacob and Jeremy Singer. 2023 “Morello MicroPython: A Python Interpreter for CHERI”. In Proceedings of the 20th ACM SIGPLAN International Conference on Managed Programming Languages and Runtimes (MPLR’23) November 23, 2023, Cascais, Portugal. – doi: [10.1145/3617651.3622991](https://doi.org/10.1145/3617651.3622991).

- P*₅ Duncan Lowther, Dejice Jacob and Jeremy Singer. 2023 “CHERI Performance Enhancement for a Bytecode Interpreter”. In Proceedings of the 15th ACM SIGPLAN International Workshop on Virtual Machines and Intermediate Languages (VMIL’23), November 23,2023, Cascais, Portugal. – doi: [10.1145/3623507.3623552](https://doi.org/10.1145/3623507.3623552).
- P*₆ Jacob Bramley, Dejice Jacob, Andrei Lascu, Jeremy Singer and Laurence Tratt. 2023 “Picking a CHERI Allocator: Security and Performance Considerations”. In Proceedings of the ACM SIGPLAN International Symposium on Memory Management (ISMM’23), June 18,2023, Orlando, USA. – doi: [10.1145/3591195.3595278](https://doi.org/10.1145/3591195.3595278).
- P*₇ Dejice Jacob and Jeremy Singer. 2022. “Capability Boehm: Challenges and Opportunities for Garbage Collection with Capability Hardware”. In Proceedings of the 18th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments (VEE’22), March 1,2022, Lausanne, Switzerland. – doi: [10.1145/3516807.3516823](https://doi.org/10.1145/3516807.3516823).
- P*₈ Stephen McQuistin, Vivian Band, Dejice Jacob, and Colin Perkins. 2021. “Investigating Automatic Code Generation for Network Packet Parsing”. In Proceedings of the 20th International Federation for Information Processing (IFIP) Networking conference (IFIP ’21). June 21-24,2020, Espoo, Finland, – doi: [10.23919/IFIPNetworking52078.2021.9472829](https://doi.org/10.23919/IFIPNetworking52078.2021.9472829).
- P*₉ Dejice Jacob, Phil Trinder, and Jeremy Singer. 2020. “Pricing Python Parallelism: a Dynamic Language Cost Model for Heterogeneous Platforms”. In Proceedings of the 16th ACM SIGPLAN International Symposium on Dynamic Languages (DLS ’20), November 17, 2020, Virtual, USA. – doi: [10.1145/3426422.3426979](https://doi.org/10.1145/3426422.3426979).
- P*₁₀ Stephen McQuistin, Vivian Band, Dejice Jacob, and Colin Perkins. 2020. “Parsing Protocol Standards to Parse Standard Protocols”. In Proceedings of the 5th Applied Networking Research Workshop (ANRW ’20), July 30,2020, New York, NY, USA, – doi: [10.1145/3404868.3406671](https://doi.org/10.1145/3404868.3406671).
- P*₁₁ Dejice Jacob, Phil Trinder, and Jeremy Singer. 2019. “Python Programmers Have GPUs too: Automatic Python Loop Parallelization with Staged Dependence Analysis”. In Proceedings of the 15th ACM SIGPLAN International Symposium on Dynamic Languages (DLS ’19), October 20, 2019, Athens, Greece, pp 42-54 – doi: [10.1145/3359619.3359743](https://doi.org/10.1145/3359619.3359743).
- P*₁₂ Dejice Jacob and Jeremy Singer. 2019. “ALPyNA: acceleration of loops in Python for novel architectures”. In Proceedings of the 6th ACM SIGPLAN International Workshop on Libraries, Languages and Compilers for Array Programming (ARRAY 2019). ACM, New York, NY, USA, 25-34 – doi: [10.1145/3315454.3329956](https://doi.org/10.1145/3315454.3329956).
- P*₁₃ Kristian Hentschel, Dejice Jacob, Jeremy Singer and Matthew Chalmers. “Supersensors: Raspberry Pi devices for smart campus infrastructure”. In 2016 IEEE 4th International Conference on Future Internet of Things and Cloud (FiCloud), pp. 58-62. IEEE, 2016 – [10.1109/FiCloud.2016.16](https://doi.org/10.1109/FiCloud.2016.16).
- P*₁₄ Dejice Jacob. “Remote control device for controlling the presentation of broadcast programming”. U.S. Patent No. [8,462,275](https://patent.google.com/patent/8462275). 11 Jun. 2013.

Research and Development Experience

Research Associate, University of Glasgow

M4Secure, (July 2023 - Present)

Automated reasoning and generation of security guarantees and proofs for memory allocators synthesised using AI Large Language Models. The allocators generated can be customised to exploit new runtime hardware security features (e.g. *CHERI* and *ARM-MTE*).

Capable VMs, (December 2020 - July 2023)

Exploiting fine-grained hardware *capabilities* of the CHERI CPU architecture to improve the software security of Virtual Machines as part of the EPSRC project *Capable VMs* (EP/V0000349/1). Our development work on BDWGC garbage collector resulted in the up-stream code being re-factored to improve support for capability architectures such as CHERI. The CHERI port of MicroPython, a python interpreter for embedded devices, showed better resilience against exploits of CVEs compared to upstream code.

Research Assistant, University of Glasgow

March 2020 - December 2020

Introducing formal verification and automatic parser generation of IETF standards from informal language specification and ASCII diagrams on EPSRC project : *Improving Protocol Standards for a more Trustworthy Internet* (EP/R04144X/1).

Software Intern, Codeplay Software Ltd, Edinburgh

October 2017 - April 2018

Characterising performance of Codeplay’s ComputeAorta LLVM based OpenCL compiler for OpenCV vision based kernels. Wrote tools to isolate execution of JIT generated OpenCV-OpenCL kernels, map execution addresses to debug symbols and analyse performance counter metrics from execution traces.

Senior Engineer, Platform Support Team, Echostar Europe

February 2008 - January 2016

Specialised in bootloaders, over-the-air firmware upgrades and board-bring up software. Developed embedded RTOS kernel space device drivers for tuners, DVB-DSMCC packet filters, and flash devices. Was also responsible for board diagnostics for supporting the manufacturing process.

**Assistant Systems Engineer, Quartz Interface Architecture, Tata Consultancy Services
September 2003 - September 2006**

Software architect for Quartz, a core-banking application of Tata Consultancy Services. Responsible for developing tools and libraries for performance optimisation of server side software.

Academic Service

- Program Committee chair for *Virtual Machines and Language Implementations* (VMIL, 2024), Pasadena, USA
- Reviewer for ACM journal *Transactions on Architecture and Code Optimization* (TACO)
- Program Committee member for *Dynamic Languages Symposium* (DLS, 2021), Chicago, USA
- Publicity chair for *Managed Programming Languages and Runtimes* (MPLR, 2021), Münster, Germany
- Reviewer for poster track at *International Conference on Distributed Computing Systems* (ICDCS, 2025), Glasgow, UK

Teaching and Supervision Experience

University of Glasgow

February 2016 - Present

- Guest lectures to MSc and graduate L4/L5 students on “Loop parallelisation in Python”, University of Glasgow (November, 2019 and March, 2020).
- Supervised three MSc projects on SIMD programming and rust based CHERI toolsets
- Co-supervised two Level 4 undergraduate student projects in WebAssembly
- Tutoring for undergraduates – Level 3 Operating Systems, Level 1 and Level 2 Programming.
- Lab demonstrator for MSc (IT) students.
- Python programming for school leaving students at University of Glasgow summer school.

Service Activities

University of Glasgow

February 2016 - Present

- **GLA**asgow Systems Section (GLASS) seminar series organiser, 2021–22.
- Network administrator for the MaRIONet project (March,2019 – March,2020). The role entailed maintaining the project website, coordinating the mailing list, promotional activities and financial administrative work.
- Organised three workshops at the SICSA PhD conference, Dundee, 2017.
- Organised outreach activities for popularisation of computing science. Volunteered to be a member of the outreach committee.