Dejice Jacob

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Objectives

A dedicated software research engineer with a solid research background and a decade of industry experience. I would like to work in a research oriented organisation that focuses on programming languages, compilers, runtimes and optimisation tools in emerging technologies like parallel computing and hardware acceleration.

Education

An engineer dedicated to continuous learning and research in the field of systems and software.

PhD, University of Glasgow
February 2016 - November 2020
EPSRC funded research titled 'Opportunistic Acceleration of Array-centric Python Computation in Heterogeneous Environments' – (doi: 10.5525/gla.thesis.82011) under the supervision of Dr. Jeremy Singer and Professor Phil Trinder, School of Computing Science, University of Glasgow. This research was done to further the goals of the EPSRC "AnyScale Apps" project (EP/L000725/1). The thesis was shortlisted as one of the four finalists for the SICSA PhD Award for Best Dissertation in Scotland, 2021.

MSc (Distinction), System Level Integration, iSLI, University of Edinburgh
October 2006 - October 2007
Taught modules included VLSI, embedded systems and DSP. My project titled "Software-Centric Design of a Network Co-processor for Embedded systems" was an industrial project developed at Critical Blue, Edinburgh.

BE, Electrical & Electronics Engineering, Regional Engineering College, Trichy, India
September 1999 - May 2003
Taught modules included embedded software, digital logic, computer architecture, electrical machines and power distribution. Final year project was the design of an active power filter to dynamically calculate and cancel impedance caused by harmonics. CGPA–7.1/10.

Publications and Patent

- Jacob Bramley, Dejice Jacob, Andrei Lascu, Jeremy Singer and Laurence Tratt. 2022 "Picking a CHERI Allocator: Security and Performance Considerations". In Proceedings of the ACM SIGPLAN International Symposium on Memory Management (ISMM'23), June 18,2023, Orlando, USA. – doi: 10.1145/3591195.3595278.
- Dejice Jacob and Jeremy Singer. 2022. "Capability Boehm: Challenges and Opportunities for Garbage Collection with Capability Hardware". In Proceedings of the 18th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments (VEE'22), March 1,2022, Lausanne, Switzerland. – doi: 10.1145/3516807.3516823.
- Stephen McQuistin, Vivian Band, Dejice Jacob, and Colin Perkins. 2021. "Investigating Automatic Code Generation for Network Packet Parsing". In Proceedings of the 20th International Federation for Information Processing (IFIP) Networking conference (IFIP '21). June 21-24,2020, Espoo, Finland, – doi: 10.23919/IFIPNetworking52078.2021.9472829.
- Dejice Jacob, Phil Trinder, and Jeremy Singer. 2020. "Pricing Python Parallelism: a Dynamic Language Cost Model for Heterogeneous Platforms". In Proceedings of the 16th ACM SIGPLAN International Symposium on Dynamic Languages (DLS '20), November 17, 2020, Virtual, USA. – doi: 10.1145/3426422.3426979.
- Stephen McQuistin, Vivian Band, Dejice Jacob, and Colin Perkins. 2020. "Parsing Protocol Standards to Parse Standard Protocols". In Proceedings of the 5th Applied Networking Research Workshop (ANRW '20), July 30,2020, New York, NY, USA, – doi: 10.1145/3404868.3406671.
- Dejice Jacob, Phil Trinder, and Jeremy Singer. 2019. "Python Programmers Have GPUs too: Automatic Python Loop Parallelization with Staged Dependence Analysis". In Proceedings of the 15th ACM SIGPLAN International Symposium on Dynamic Languages (DLS '19), October 20, 2019, Athens, Greece, pp 42-54 – doi: 10.1145/3359619.3359743.

- Dejice Jacob and Jeremy Singer. 2019. "ALPyNA: acceleration of loops in Python for novel architectures". In Proceedings of the 6th ACM SIGPLAN International Workshop on Libraries, Languages and Compilers for Array Programming (ARRAY 2019). ACM, New York, NY, USA, 25-34 – doi: 10.1145/3315454.3329956.
- Kristian Hentschel, Dejice Jacob, Jeremy Singer and Matthew Chalmers. "Supersensors: Raspberry Pi devices for smart campus infrastructure". In 2016 IEEE 4th International Conference on Future Internet of Things and Cloud (FiCloud), pp. 58-62. IEEE, 2016 – 10.1109/FiCloud.2016.16.
- Dejice Jacob. "Remote control device for controlling the presentation of broadcast programming". U.S. Patent No. 8,462,275. 11 Jun. 2013.

Research and Development Experience

Research Associate, University of Glasgow
December 2020 - Present
Exploiting fine-grained hardware *capabilities* of the CHERI CPU architecture to improve the software security of Virtual Machines as part of the EPSRC project *Capable VMs* (EP/V0000349/1) project.

Research Assistant, University of Glasgow
March 2020 - December 2020
Introducing formal verification and automatic parser generation of IETF standards from informal language specification and ASCII diagrams on EPSRC project : *Improving Protocol Standards for a more Trustworthy Internet* (EP/R04144X/1).

Software Intern, Codeplay Software Ltd, Edinburgh
October 2017 - April 2018
Characterising performance of Codeplay's ComputeAorta LLVM based OpenCL compiler for OpenCV vision based kernels. Wrote tools to

- isolate execution of Just-in-Time generated OpenCV-OpenCL kernels from the online compiler's own execution to extract metrics from *linux-perf*.
- map the performance counter absolute code address generated by *linux-perf* with the code symbols and relative addresses generated by the online OpenCL LLVM compiler.
- classify and cluster different performance counter metrics for each computation kernel.

Senior Engineer, Platform Support Team, Echostar Europe
February 2008 - January 2016
Specialised in bootloaders, over-the-air firmware upgrades and board-bring up software. Developed embedded RTOS kernel space device drivers for tuners, DVB-DSMCC packet filters, and flash devices. Was also responsible for board diagnostics for supporting the manufacturing process.

Assistant Systems Engineer, Quartz Interface Architecture, Tata Consultancy Services
September 2003 - September 2006
Software architect for Quartz, a core-banking application of Tata Consultancy Services. Responsible for developing tools and libraries for performance optimisation of server side software.

Teaching Experience

University of Glasgow
February 2016 - Present
- Tutoring for undergraduates – Level-3 Operating Systems and Level-1 and Level-2 Programming.
- Lab demonstrator for MSc (IT) students.
- Python programming for school leaving students at University of Glasgow summer school.

Academic Service

- Program Committee member for *Dynamic Languages Symposium* (DLS, 2021), Chicago, USA

- Publicity chair for *Managed Programming Languages and Runtimes* (MPLR, 2021), Münster, Germany

Administrative Experience

University of Glasgow
February 2016 - Present

- **GLA**asgow **S**ystems **S**ection (GLASS) seminar series organiser, 2021–22.
- Network administrator for the MaRIONet project (March,2019 – March,2020). The role entailed maintaining the project website, coordinating the mailing list, promotional activities and financial administrative work.
- Organised three workshops at the SICSA PhD conference, Dundee, 2017.

Skill Set

- Excellent low-level assembler (MIPS) and C, C++ and Python
- Knowledge of LLVM compiler stack
- Excellent knowledge of GPU programming in OpenCL (C-dialect) and CUDA
- Extensive knowledge and experience of multi-threaded programming and various IPC mechanisms on POSIX systems.
- Very Proficient in Shell scripting (bash) and build systems on Linux development platforms
- Good understanding of various hardware bus protocols like I2C, SPI, HDMI, 802.3 ethernet.
- Excellent understanding of Recovery bootloaders and downloaders for Set-top-Boxes
- Implementing embedded low memory footprint network stacks and writing minimal low-level device drivers for recovery boots and single/multi-thread no-OS applications or RTOS based applications.
- Very good Low Level device driver/BSP[1] development skills.

[1] Board Support Package

Conferences and Presentations

- Invited seminar about "ALPyNA" loop parallelisation at Programming Languages and Systems Research Group, University of Kent (February, 2021).
- Attended Google Compiler Summit, Munich (December, 2019 and December, 2020).
- Guest lecture to MSc and graduate L4/L5 students on "Loop parallelisation in Python", University of Glasgow (November, 2019 and March, 2020).
- Presentation of Python loop parallelisation efforts – ALPyNA at 4^{th} UK Systems Research workshop, Newcastle (March, 2019).
- Presentation of Python loop parallelisation at the "Adaptive Many-Core Architectures and Systems Workshop", York (June, 2018).
- Participated in the HiPEAC Heterogeneous Programming challenge, 2017.
- Invited seminar about "AnyScale Applications" at the Computer Languages group, Technical University of Vienna (July, 2016).
- Attended the HiPEAC ACACES summer school, Fiuggi (July, 2016). I attended workshops on *(i)* Superscalar architectures *(ii)* GPU programming optimisations and *(iii)* Using the Polyhedral model in loop optimisation.
- Attended the LLVM and GNU Tools Cauldron. Hebden Bridge (August, 2016).
- Attended the Virtual Machine Summer School (VMSS'16), Windsor (May, 2016).

References

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Prof. Phil Trinder, University of Glasgow
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