Mapping Irregular MPSoC Topologies onto 2D-meshes
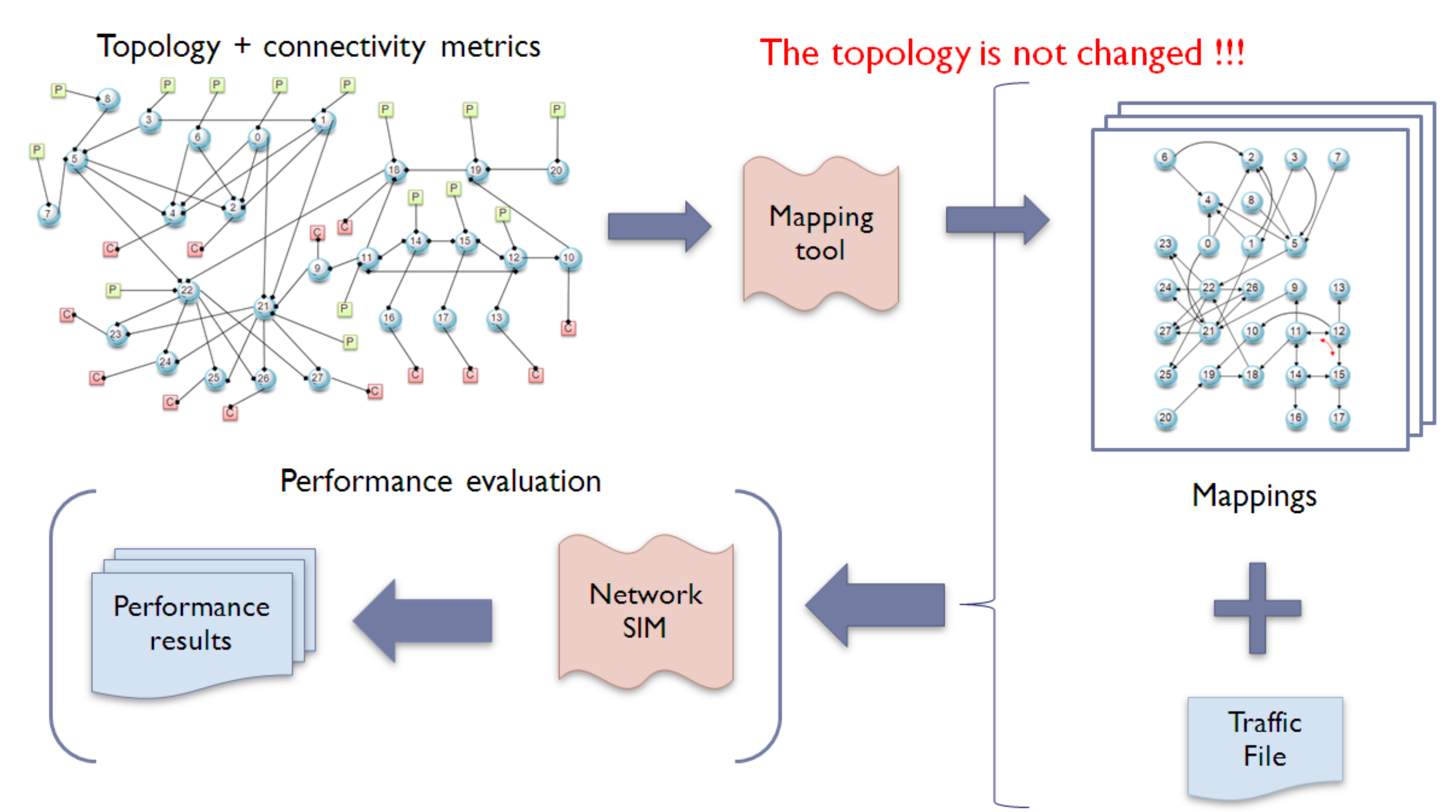
José Cano, José Flich, José Duato
Universitat Politècnica de València

Marcello Coppola, Riccardo Locatelli
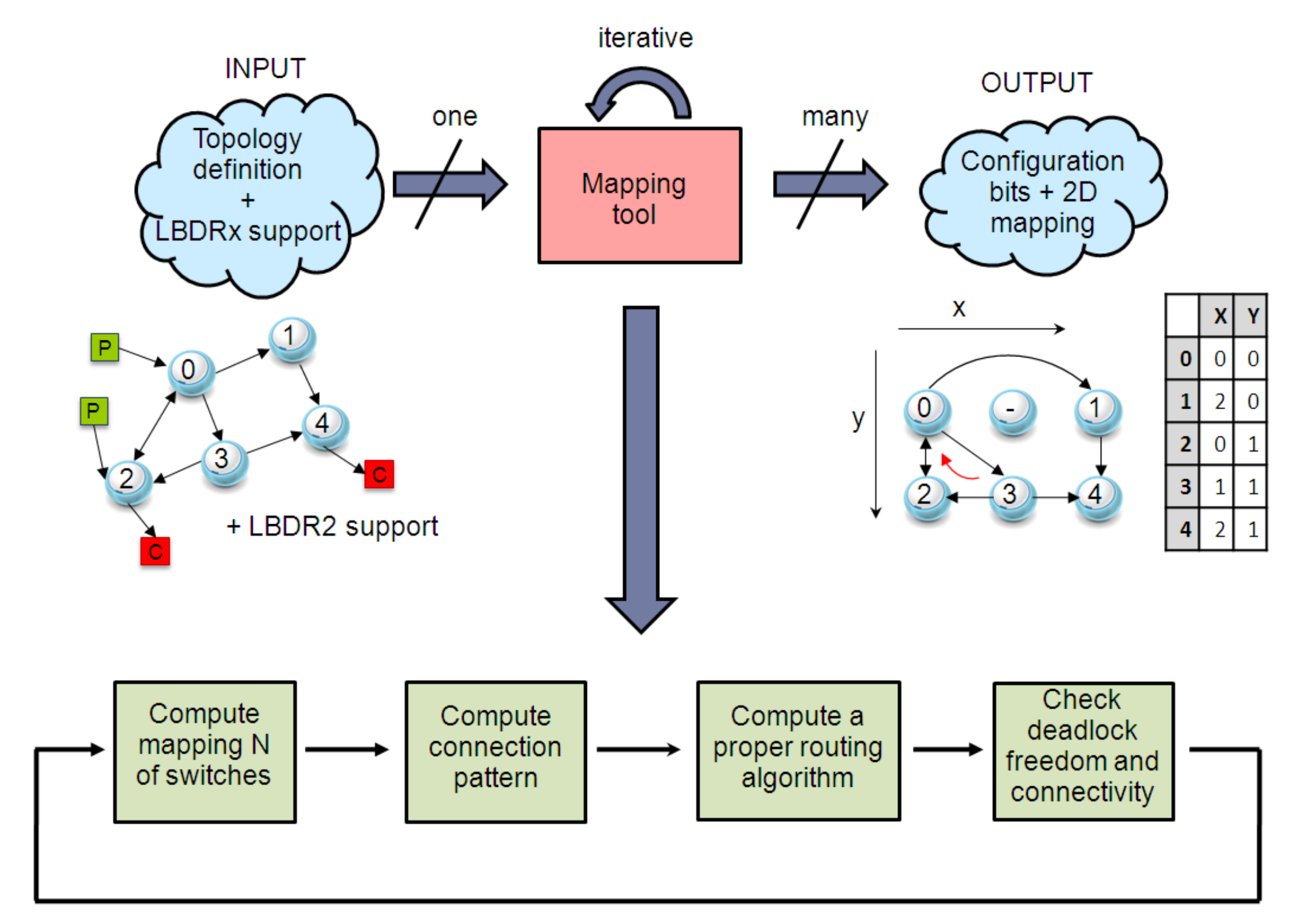STMicroelectronics

1. Introduction

In application-specific SoCs the topology is usually irregular. We present a mapping tool able to map the initial irregular topology of a SoC system into a logical regular structure (2D-mesh) where a Logic-Based Distributed Routing mechanism (LBDRx) can be applied. The goal is to implement the routing paths without using memory resources. The original topology is not changed. Evaluation results show the effectiveness of the mapping tool.

2. Overall scheme

3. Foundations

Routing bits

Connectivity bits

Extended Logic-Based Distributed Routing (LBDRx)

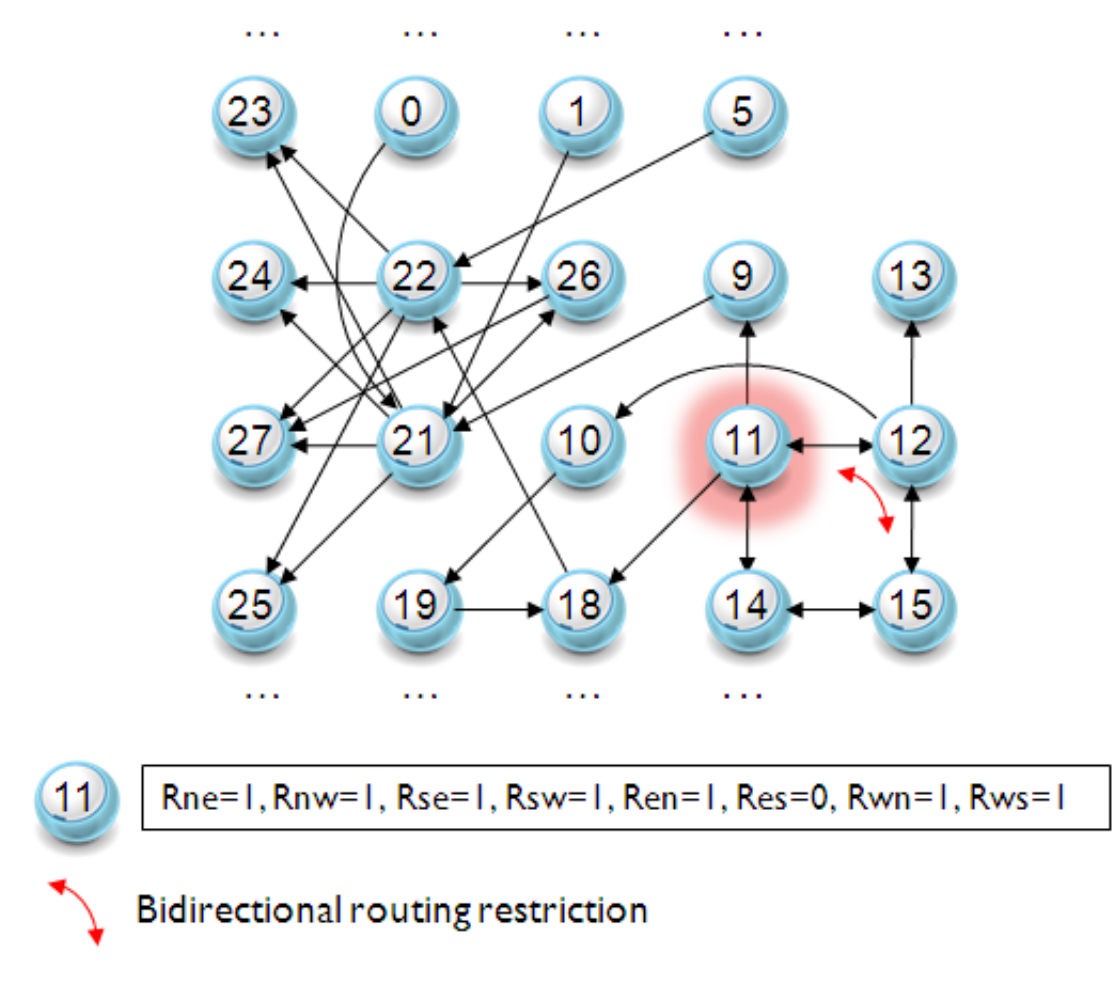### Non-minimal path support: Deroutes

4. Mapping tool

The tool is adapted to different versions of LBDRx. It takes as an input the topology and the type of LBDRx support and outputs (for every possible solution) the set of configuration bits together with the mapping coordinates of every switch into a 2D grid. It is worth highlighting that the mapping tool does not physically change the topology, indeed it only logically maps the topology onto a 2D grid.
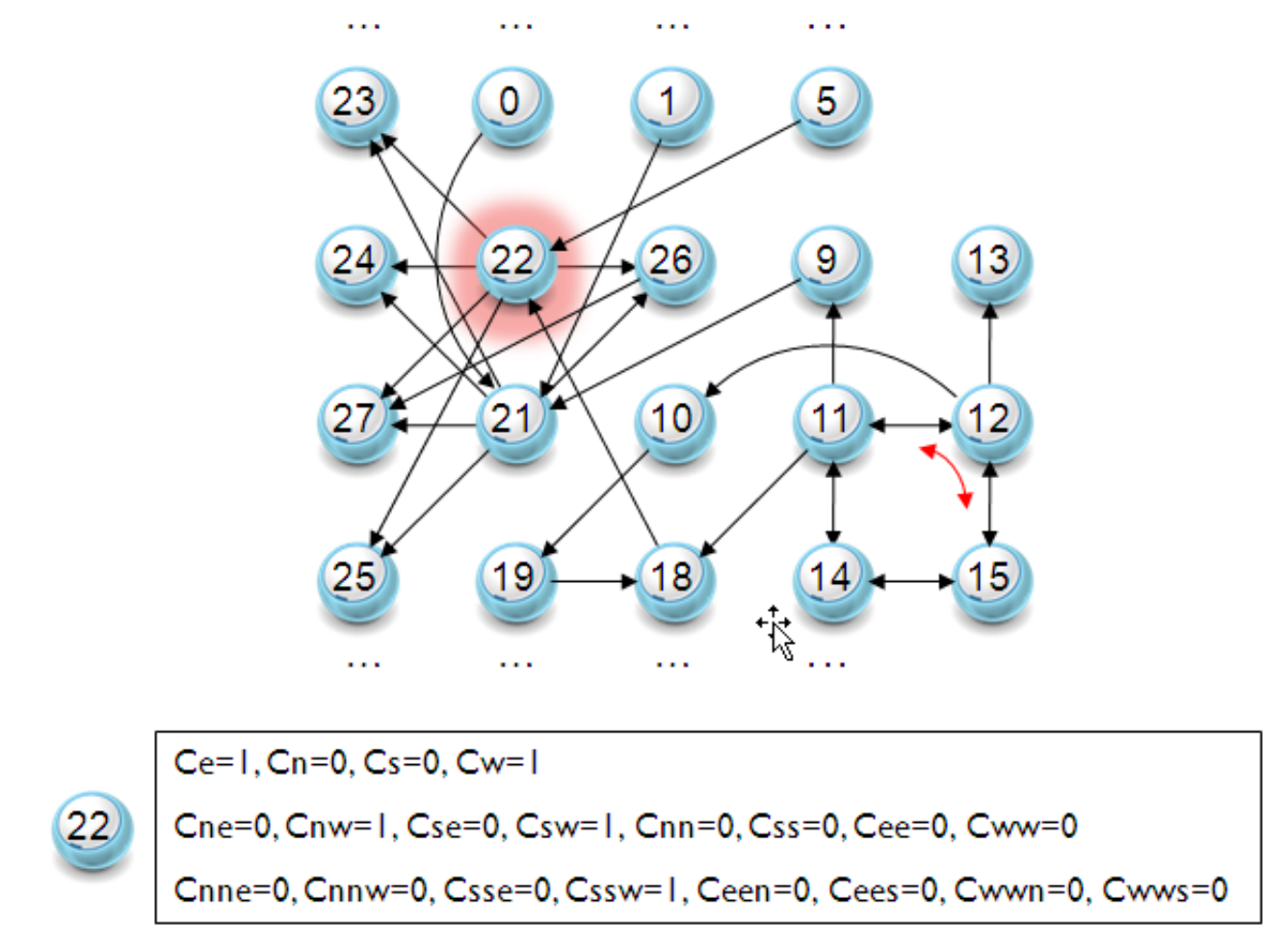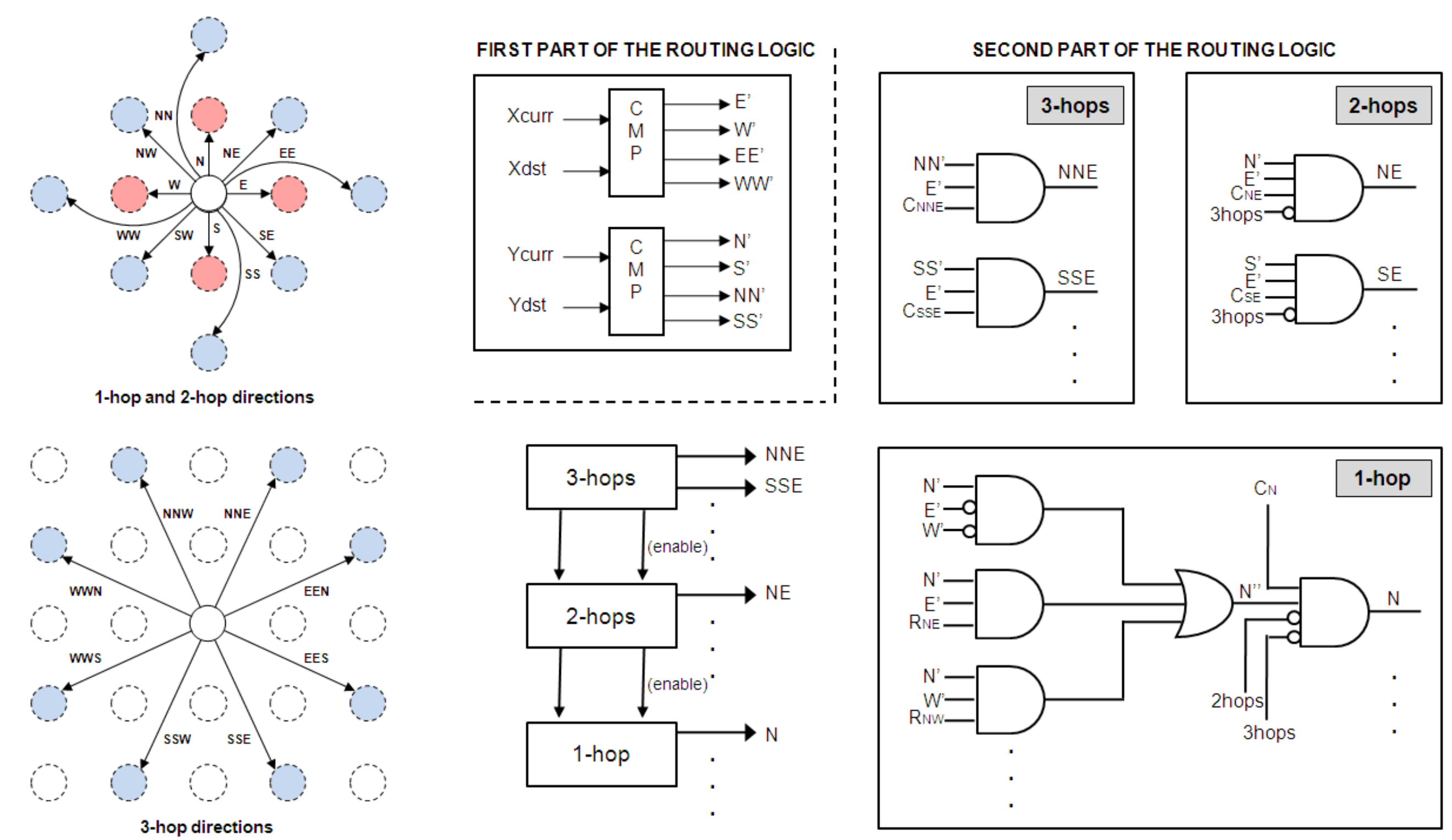

5. Evaluation

A. Mapping tool analysis

We used several sets of sample topologies with increasing complexity. The main purpose was to measure the number of correct mappings generated for every analyzed topology and the time required to complete the procedure.
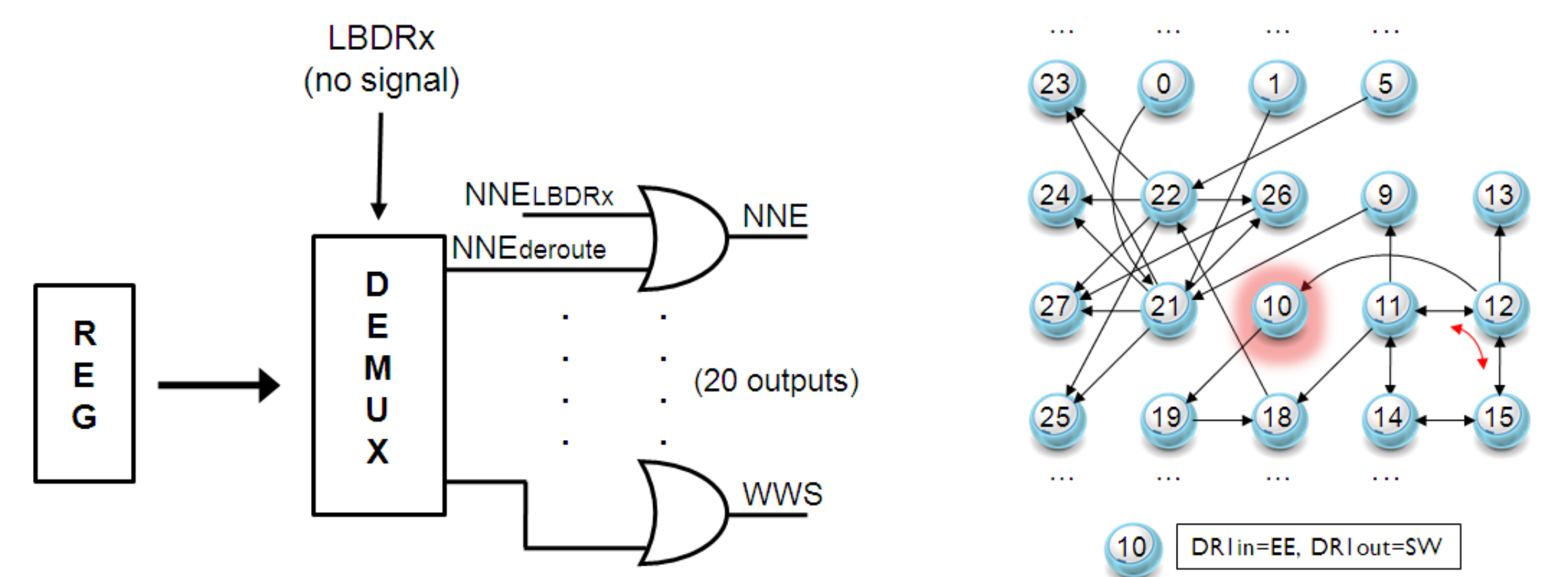
Topology	Grid size	Correct	Deroutes	Time
Type 1	4x4	> 10.000	not needed	3-5 min
Type 2	5x5	> 100.000	not needed	10-15 min
Type 3	5x6	> 100.000	not needed	30-45 min
Type 4	5x7	> 100.000	10-15	1-2 hours
Complex case	5x7	578.952	13-15	2 hours

- Run in: AMD Opteron (2,8 Ghz dual core, 8Gb RAM)
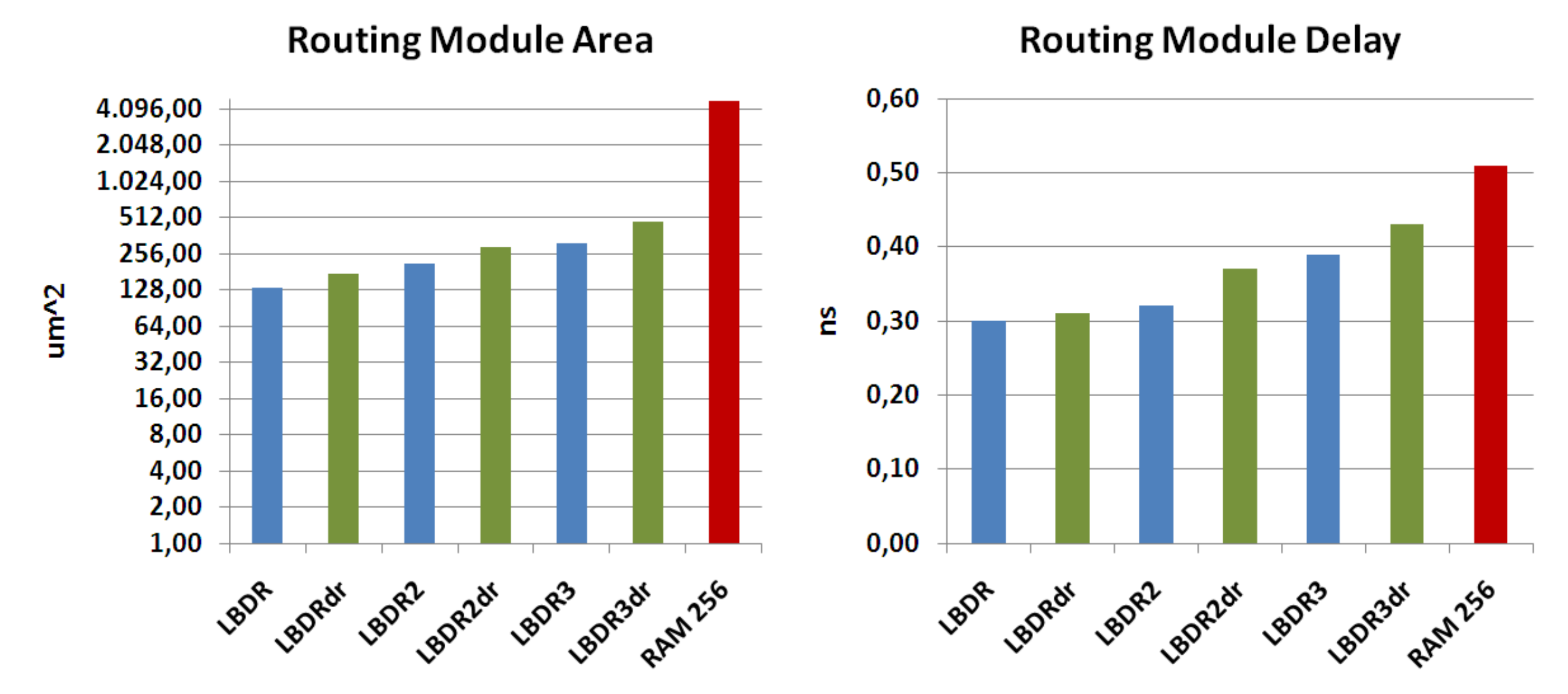
B. LBDRx vs Routing tables

We observe that the differences between all the LBDRx versions are slight in terms of both area and delay. When compared with a RAM memory of 256 entries, the LBDRx version are much compact. For delay, although similar, the LBDRx versions have lower access latency.

- LBDRx versions designed and synthesized with 45nm Nangate opensource library

- Routing tables of 256 entries using Memaker

6. Conclusion

We have presented a mapping tool able to obtain different mappings of the same irregular topology onto a 2D grid. The tool is key for the application of the LBDRx mechanism. The provided results demonstrate the applicability of the mapping tool onto a wide set of topologies. In all cases, a valid mapping was achieved. As future work we plan to focus on performance issues. Different mappings may end up in different performance numbers.