CHERI Compartments

Toward Transient-Execution Attack Mitigations on CHERI Compartments

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Transient-Execution Attacks

Transient-execution attacks combine:

- Directed speculative execution
- Side-channels, e.g., cache timing

Spectre v1 is most infamous example:

```
if (idx0 < size){
        int idx1 = array0[idx0];
        int idx2 = array1[idx1];
        …
}
```

Cache lines for `array1`

Transient-Execution Attacks

Transient-execution attacks have become numerous:

- Spectre-like: Following control-flow or data-flow misprediction
- Meltdown-like: Following a faulting instruction
- MDS (Microarchitectural Data Sampling): Leaking in-flight data from buffers

Leakage sources and reasons:

- Branch direction prediction
- Indirect jump target prediction
- Return address prediction
- Memory disambiguation
- Speculative load forwarding
- Instruction scheduling
- Out-of-order execution
- Reading from store buffers
- …

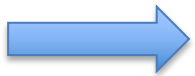
Transient-Execution Attacks on CHERI

Previous research shows that CHERI systems can be vulnerable to transient-execution attacks

- Traditional Spectre attacks mostly work
- CHERI can, but does not need to protect against transient-execution attacks

	CHERI-RISC-V
Spectre-PHT	Safe
Spectre-BTB	Vulnerable
Spectre-RSB	Vulnerable
Spectre-STL	Vulnerable
Meltdown-US-CHERI	Safe
Meltdown-GP-CHERI	Safe

Results on obtained on CHERI-Toooba

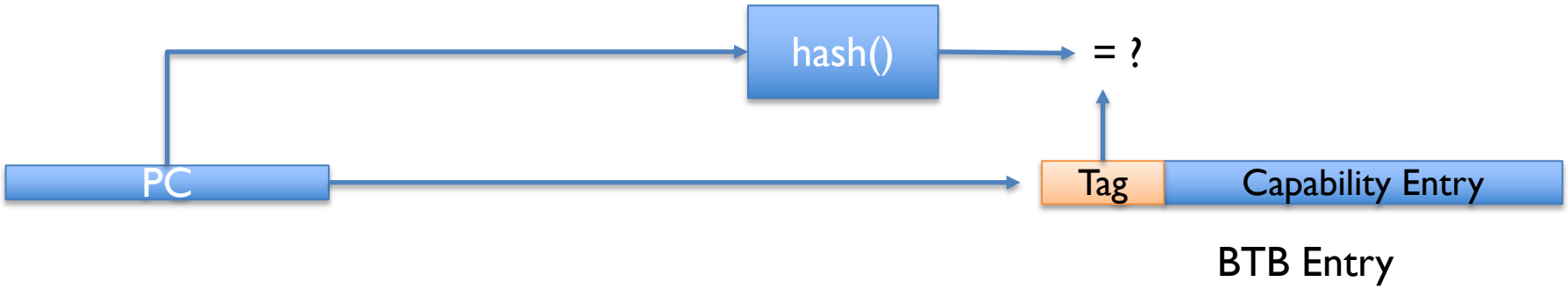


Mitigation of transient-execution attacks is caused by design properties of CHERI-Toooba rather than CHERI

Transient-Execution Attacks on CHERI

What are the reasons for the successful attacks on CHERI systems?

"Speculation with capabilities"



Malicious code retrieves a capability and all its permissions during speculative execution!

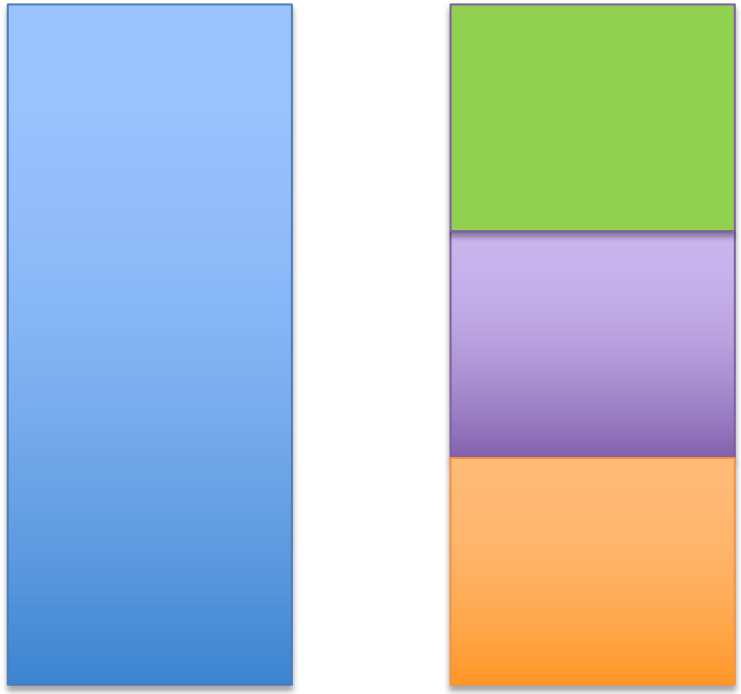
How to mitigate transient-execution attacks?

Compartmentalisation

Conventional compartmentalisation:

- Privilege decomposition
- Traditionally separate one process into multiple compartments with less privileges each
- Decrease the attack surface

→ Malicious code cannot escape their compartment



Big process

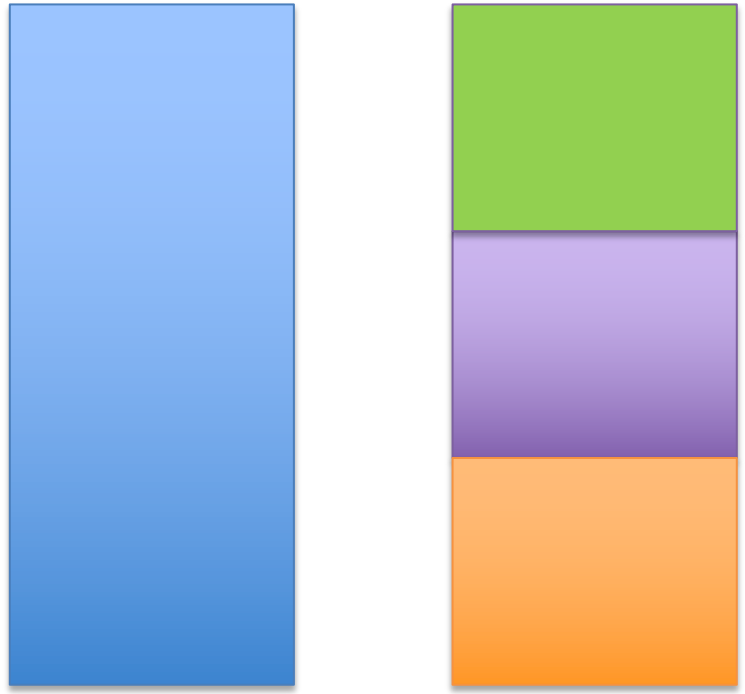
Multiple small compartments

Compartmentalisation against Transient Execution

Effective mitigation approach, but:

- Coarse-grained approach does not allow for fine-grained protection
- High performance cost when process switching

We need to do better!



Wild speculation

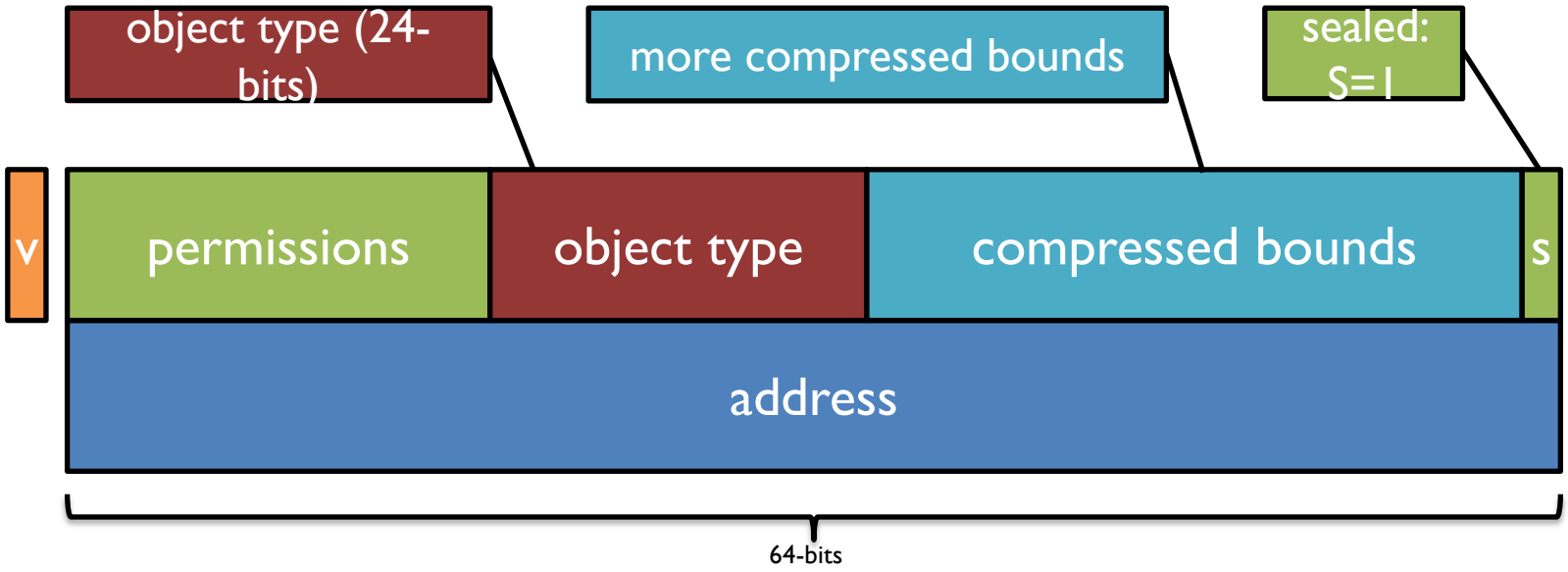
No state sharing between compartments

Compartmentalisation with CHERI

Advantages against conventional compartmentalisation:

- Fine-grained decomposition
- Built-in domain transitions, e.g., through capability sealing (non-dereferencable capabilities)

That sounds like the problem is already solved!



What are the main challenges ahead?

Compartmentalisation Challenges (1)

"The architectural specification vacuum"

Currently, the architecture does not constrain speculative execution

We need architectural guarantees about speculative execution for security

Guarantees needed for:

- Ability to test hardware for security properties
- Build secure software on top of architectural guarantees

Compartmentalisation Challenges (2)

"Understanding what we need to protect"

High-end microarchitectures have more and more state (Apple M1 has 16 billion transistors as an indicator for microarchitectural state growth)

Different forms of state:

- Long-term (i.e., BTB)
- Transient (i.e., scheduling in a pipeline)

Reason for complexity:

Need for ever increasing single-core performance!

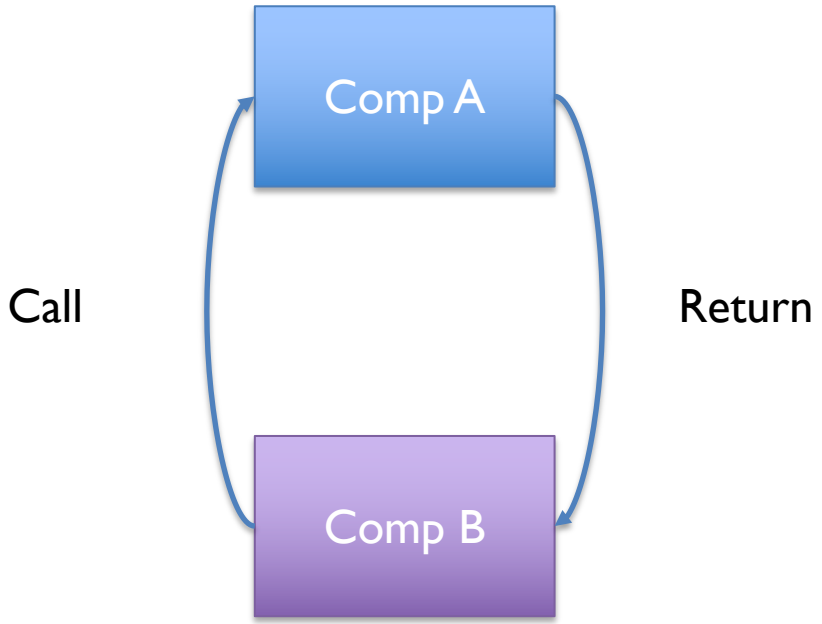
We need a full microarchitectural audit!

Compartmentalisation Challenges (3)

"How to implement a compartment?"

Hardware design challenges:

- Large increase in compartment switches due to fine-grained compartments
- Every compartment switch is more expensive than a function call
- State sharing can benefit performance
- Dedicated additional microarchitectural state for compartments needed



Calls and returns need to be inexpensive

Compartmentalisation Challenges (4)

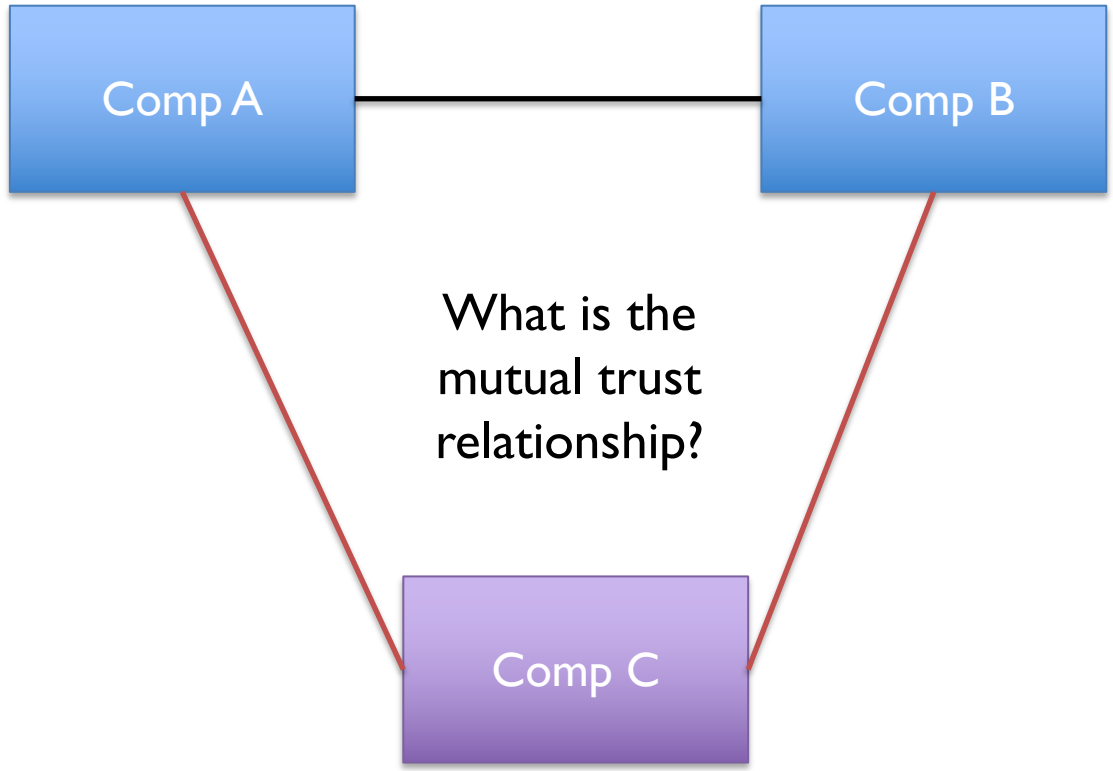
"How to implement security?"

Security challenges:

- Multiple different security models
- Hierarchy of compartments
- Trust relations between compartments

The two compartments have the same code

The two compartments have different code



Conclusions

- Compartmentalisation is needed to mitigate transient-execution attacks
- Industry solutions are performance expensive and coarse grained
- CHERI allows fine-grained compartmentalisation
- Research in progress:
  - Architectural specification necessary
  - Identifying relevant microarchitectural state
  - Implementing microarchitectural solutions