A Hardware Relaxation Paradigm for Solving NP-Hard Problems

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Abstract

Digital circuits with feedback loops can solve some instances of NP-hard problems by relaxation: the circuit will either oscillate or settle down to a stable state that represents a solution to the problem instance. This approach differs from using hardware accelerators to speed up the execution of deterministic algorithms, as it exploits stabilisation properties of circuits with feedback, and it allows a variety of hardware techniques that do not have counterparts in software. A feedback circuit that solves many instances of Boolean satisfiability problems is described, with experimental results from a preliminary simulation using a hardware accelerator.

Keywords: NP-hard problem, Boolean satisfiability, digital circuit with feedback, relaxation, simulated annealing

1. INTRODUCTION

NP-complete problems lie on the boundary of what is economically computable. They are effectively computable on a Turing Machine, but their worst-case run times are believed to grow exponentially with problem size. This can make large instances of NP-complete problems too expensive for us to obtain solutions. It is suspected, but not proven, that no polynomial time algorithm exists for NP-complete problems, and that if a deterministic algorithm rather than an oracle is used to obtain the solution, then in the worst case the algorithm must perform an exhaustive search through a solution space whose size is an exponential function of the input size.

There have been numerous recent proposals to overcome the barrier of effective computability in computation, and proposals [5, 6, 11, 15] have been put forward for *hypercomputers* that could compute functions which are uncomputable on a Turing machine. The feasibility of building such devices remains in dispute [7, 25, 33, 8].

A related question concerns the time complexity of computable functions. Many models of computation are mathematical state machines that are provably equivalent to a Turing Machine, but some physical systems that can perform computation have not been proven to be Turing equivalent, either in terms of computability or time complexity. Do there exist physical systems that can solve computable problems with a lower time order than a Turing Machine?

A particularly significant type of physical computation system is a circuit comprising Boolean logic gates and (possibly) flip flops. Such circuits are normally designed according to a strongly disciplined synchronous style in order to keep their behaviour simple, digital, and predictable. Synchronous circuits behave like mathematical state machines. However, unconstrained Boolean networks with feedback can exhibit a variety of complex behaviours, including non-digital behaviour such as metastability [36]. Given constant inputs, a circuit may stabilise, it may settle down into an oscillation among a set of states, or it may fluctuate chaotically.

Kauffman has shown [20] that random Boolean networks of size n have expected median state cycle lengths of $O(\sqrt{n})$. Thus a system with a very large state space (e.g. $2^{10000} \approx 10^{3000}$) may settle down and cycle among a quite small number of states (e.g. 100).

In this paper we investigate the computational complexity of Boolean networks with feedback for solving instances of Boolean Satisfiability (SAT), a standard NP-complete problem. We show how to compile (in polynomial time) an instance of SAT into a circuit whose fixed point (where the signals remain stable) represents a solution to that problem instance. The circuit may not reach a fixed point; oscillation among a set of states constitutes a failure to solve the problem instance. Kauffman's result suggests that there is a reasonable probability that such a circuit will indeed solve the instance. We have experimented with a prototype of the system, using FPGA technology to simulate the general class of circuit we define. Preliminary experimental results show that the approach does indeed solve many SAT problem instances quickly.

In Section 2 we consider the problem of Boolean satisfiability, and Section 3 reviews existing solvers. Section 4 outlines an ASIC (application-specific integrated circuit) design that can solve problem instances by relaxation, and we show how to compile an arbitrary instance of SAT in order to run on the circuit. Section 5 discusses initial results obtained by a hardware simulator, and Section 6 concludes.

2. THE PROBLEM DOMAIN: BOOLEAN SATISFIABILITY (SAT)

The problem domain we consider is Boolean satisfiability. Given an arbitrary Boolean expression over a set of variables, the problem is to determine whether there exists a set of variable settings (to true or false) that makes the entire expression true. A specific Boolean expression is called an *instance* of the general problem. We restrict the Boolean expressions to a canonical form: the logical conjunction of clauses, where each clause is the logical disjunction of one or more literals, and a literal is either a variable or the negation of a variable. This restricted version of Boolean satisfiability is called SAT, and it is also NP-complete. For example, the following expression is an instance of SAT:

$$(a \vee \neg d \vee e) \wedge (d \vee e \vee f) \wedge (b \vee \neg c \vee \neg d)$$

Although SAT is an NP complete problem, not all instances of it are hard to solve. Previous research has shown that the set of SAT problems has an interesting structure, with a phase change from a subset of problems with few solutions to a subset of problems with many solutions [19, 18, 37]. The instances of SAT that are hard lie mostly near the phase change. This previous research is experimental: large sets of problem instances are generated randomly and their solution times measured.

Cheeseman, Kanefsky and Taylor observed an abrupt phase transition from solubility to insolubility in graph colouring problems as average degree was increased [4]. A complexity peak was observed at this transition, and it was conjectured that this would be algorithm independent and common to all NP-complete problems. Graph colouring problems were mapped to SAT and the same phenomenon was observed, i.e. an abrupt phase transition with a corresponding complexity peak. Later studies showed that incomplete algorithms also experience the complexity peak when applied to satisfiable instances: easy solvable instances are easy, hard soluble instances are hard, and rare soluble instances found within the easy insoluble region are also easy. Much research has been done to pin down the location of the SAT phase transition and to develop theories about the location of this phase transition for problems that are NP-complete [13] or in higher complexity classes (such as quantifies SAT (QSAT)). Research to date appears to confirm that the complexity peak is indeed independent of the algorithm, and it is an open question whether physical systems that do not implement mathematical state machines have the same properties.

3. RELATED WORK ON SAT SOLVERS

Because of its theoretical interest and its practical importance, there has been extensive work on solvers for SAT.

3.1. Software solvers

There are two broad classes of SAT solvers: complete and incomplete. Complete solvers are guaranteed to find a solution if one exists and to terminate on unsatisfiable instances. They typically use a backtracking search based on the DPLL (Davis, Putnam, Logemann, and Loveland) algorithm. State of the art solvers, such as Zchaff2004 [24], MiniSAT [10, 12, 34] and BerkMin [14] employ relevance bounded learning, intelligent backjumping, and dynamic variable ordering heuristics along with smart data structures such as watched literals.

Incomplete solvers typically use a neighbourhood search algorithm, and often operate as hill climbers (or descenders). Given complete or partial setting of the variables, the settings are improved by making local changes. Solvers such as WalkSat [21] (and its predecessor GSAT) have features that are similar to Tabu search. Heuristics for optimisation strategies are discussed in [9], and runtime distributions of SAT solvers are reviewed in [16]. The algorithms for WalkSat and GSAT are shown below:

```
procedure WalkSat
   input f: array[1..c] of clauses {in CNF}
   output v:array[1..n] of boolean {a variable assignment that satisfies f}
begin
   for a := 1 to MaxTries do
      v := random truth assignment;
      for b := 1 to MaxFlips do
         if all f are true given v then return Success;
         choose a random clause cl in f such that cl=false;
         if random(0..1)<p then
            j := a random variable that appears in cl
         else
            j:= the variable in cl that will produce the biggest
                   increase in satisfied clauses when flipped
         v[j] := not v[j];
   return Fail;
end;

Procedure GSAT
   input f: array[1..c] of clauses {in CNF}
   output v:array[1..n] of boolean {a  variable assignment that satisfies f}
begin
   for a := 1 to MaxTries do
      v := random truth assignment;
      for b := 1 to MaxTries do
         if all f are true given v then return Success;
         else
            PossFlips := set of vars which increase SAT most
            j := a random element of PossFlips
            v[j] := not v[j]
   return Fail;
end;
```

State of the art SAT solvers are highly optimised pieces of code. Practical applications of SAT solvers include scheduling problems, planning (for example, in interplanetary space within Deep Space 1), configuration problems, hardware design and verification, and cryptanalysis of hash functions. SAT instances solved to date contain some hundreds of thousands of variables and millions of clauses, typically taking a handful of hours to solve.

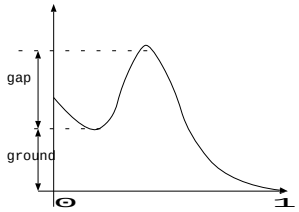

FIGURE 1: We can consider each variable to be subject to a local potential which varies according to whether the variable is true or false. To transition between Boolean values the variable has to use thermal noise to overcome a potential barrier separating the two states.

3.2. Hardware acceleration of SAT solvers with FPGAs

There has also been extensive work on using FPGAs to accelerate satisfiability algorithms. Many of these projects use FPGAs to accelerate components of the Davis-Putnam algorithm. Skliarova and Ferrari give a survey [32]; specific projects include [3] [38] [27] [1] [39] [2] [26] [31] [28] [35] [29] [40] [30].

Our approach differs from previous work in several key respects. It has an efficient polynomial time compilation of a problem instance onto the circuit; it uses relaxation rather than an algorithmic state machine to attempt to solve the instance; it uses a parallel randomised approach rather than the Davis-Putnam algorithm; it uses hardware techniques that have no counterpart in software, including pulse logic, asynchronous timing, and the use of noise to generate random numbers.

4. A HARDWARE RELAXATION PARADIGM FOR A FAST INCOMPLETE SOLVER

We now describe a new form of circuit that is capable of implementing an incomplete solver for an arbitrary instance of SAT, provided that the instance is not too large to fit on the chip. The circuit is structured as a programmable regular array of logic elements, related to but distinct from PLA, PAL, and FPGA logic, and it is suitable for implementation on an ASIC (application specific integrated circuit). In addition to the generic circuit, we describe a simple polynomial time method for compiling an arbitrary SAT instance instance to run on the circuit.

The approach is similar to simulated annealing [22] with a local potential energy function for each variable (Figure 1). The energy for the 0 or 1 states of a variable will be a function of the number of unsatisfied Boolean terms in which the variable participates. Since the number of unsatisfied terms depends on the states of other variables, the flipping of one variable will shift the energies of other variables.

A potential barrier separates the energies associated with the 0 and 1 states of a variable. At indeterminate moments, thermal noise will cause variables to flip state, and the probability that a flip will occur is an inverse function of the potential barrier. We can arrange the potentials so that the probability of a flip occurring to a variable will be zero if all the terms which contain that variable are satisfied. Once all terms have been satisfied, the system will be in a global energy minimum.

Our aim is to design an electronic circuit that can, in polynomial time, be configured to exhibit these dynamical properties for any SAT instance (up to some given size). Since chips are two dimensional and since SAT problems have two characteristic dimensions : t Boolean terms and n variables, there is in principle a good match between the two. An obvious approach is to arrange the chip as an array with each of the t terms constituting a row and each of the n variables a column (Figure 2). Each row must be able to represent an arbitrary Boolean term that has to be satisfied.

In order to configure a row as a particular Boolean term we select which variables participate in the term, and also whether the the variable is complemented. Therefore an arbitrary term in

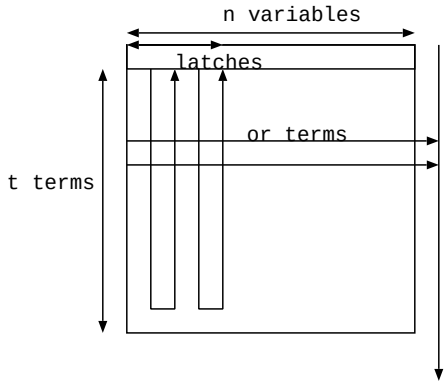

FIGURE 2: The layout is a regular two dimensional array with t terms (corresponding to the rows) and n variables (corresponding to the columns)

n variables could be encoded in $2n$ bits. Each of the t terms is represented by a shift register of length $2n$ bits. A simple option would be to concatenate these configuration shift registers into one long shift register of length $2nt$. Given a SAT problem instance in the form of a product of sums, then generating a two dimensional array of configuration bits can be computed in polynomial time on a standard computer. The computer can then shift the configuration array onto the chip, also in polynomial time.

The flip columns can be implemented as wired ORs, and ensure that the flip probability is an increasing function of the number of unsatisfied terms into which a variable enters. This models our original requirement that the flip probability should be an inverse function of a potential barrier, which is itself an inverse function of the number of unsatisfied terms using a variable. A t input AND gate along one side of the chip can detect when all terms are satisfied. Judicious design of the thermal noise source can mimic the effect of cooling a required by simulated annealing.

4.1. Structure of the programmable array circuit

Figure 3 gives an overview of the circuit. The current value of each of the Boolean variables is carried on two vertical lines (one giving the variable's value, the other its complement). There is a horizontal line that calculates the value of each term (these are the horizontal lines that have $\times$ at some of the intersections, and which terminate at an or gate symbol). This line calculates the logical disjunction of the values carried by vertical lines that have a $\times$ at the intersection; if its value is true, then the term is satisfied by the current variable settings. That signal is inverted, producing a signal whose meaning is "this term is *not* satisfied", which is then transmitted to the left on a second horizontal line. If the "not satisfied" signal is true, one or more of the variables appearing in the term must be wrong. The circuit labelled "?" controls the probability that one of these variables will be changed, and the result is carried up to the top of the circuit on another vertical signal. For example, the variable a is carried downwards on two signals (one for a, one for $\neg a$, and the "a may be wrong" signal a^W is carried back up. The circuit labelled *fix* takes the current variable value, and flips it if the variable is "wrong". The circuit is programmed to solve a specific instance of SAT by determining where the $\times$ and "?" connections are made. Those connections are controlled by flip flops, enabling the circuit to be reconfigured rapidly.

Figure 4 shows in more detail a portion of a possible term-line design, including the intersection between the horizontal term-line and two variables A and B on vertical lines. A 4 bit register (shown as 1) selects whether each variable or its complement enters into the term. This is organised as a shift register, so that the settings can be loaded efficiently into the chip. Each variable is represented by true (2) and complement (3) columns. Associated with each variable is a 'flip' column (5), which when activated will cause a set/reset latch at the top of the column to flip, changing the current state of the variable. Three input *and* gates (4) act to pull up the flip column if all of the following hold:

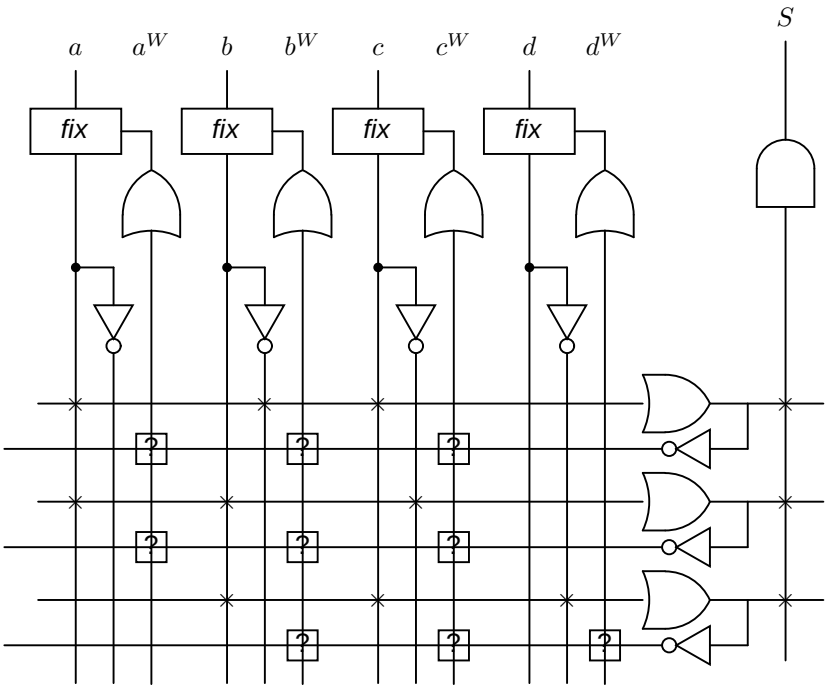

FIGURE 3: A circuit with feedback that attempts to satisfy $(a \vee \neg b \vee c) \wedge (a \vee b \vee \neg c) \wedge (b \vee c \vee \neg d)$. The circuit's behaviour is parameterised by three black box circuits, labeled *fix*, $\times$, and ?. The output S is 1 if the current values of the variables satisfy the expression. If the expression is not satisfied, the feedback loop changes values and continues trying. The behaviour of the circuit depends on the black box *fix* circuit.

1. the term (7) is currently unsatisfied;
2. the variable is selected as part of the term by the shift register;
3. a thermal noise output (6) is true.

4.2. A tunable digital noise-based random generator

Rather than using traditional pseudo-random numbers, several hardware techniques are available to improve the efficiency of the randomisation. A train of random pulses can be used instead of random integers to control the toggling. The pulse train can be generated using noise, and probabilities can be combined using a logical and-gate. The generator must produce a spike train with a random delay between subsequent spikes, and the spikes must be wide enough to toggle a latch. The average delay between subsequent spikes (called the ”period”) must be controllable. Ideally, the period will grow exponentially longer over the duration of a 3SAT search. We propose to vary the supply voltage of the circuit over time along a negative exponential:

$$V_{DD} = V_{DD_{min}} + \left(V_{DD_{max}} - V_{DD_{min}}\right) \times e^{-\frac{t}{\tau}}$$

where τ is the time constant of the system. This behaviour is easily obtained as the response of a step function to an RC filter. The actual random generator is based on a ring oscillator circuit. We exploit the well-known high-jitter behaviour of this type of oscillator to create random pulses, simply by XOR-ing two subsequent nets (Figure 4.3).

Because of the jitter, the XOR output will be a pulse of varying width, including zero-width. By low pass-filtering this signal and then recovering it, we obtain a random pulse train. The frequency of a ring oscillator is proportional to the VDD. An accurate model for the jitter of a ring oscillator is presented in [17]. Using this model it is possible to design a circuit that will generate a pulse with a probability p at a frequency governed by the VDD of the oscillator.

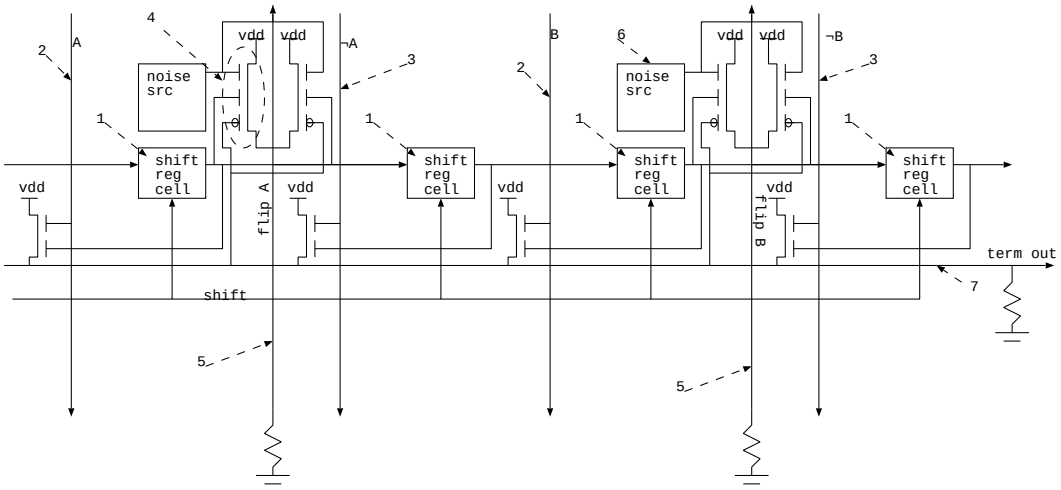

FIGURE 4: This diagram shows the intersection between two variables (labeled A,B) and a Boolean term. Corresponding to each variable are two vertical lines for the true and complement values of the variable. Configuration information in shift register cells records whether the true or complement of the variables or neither are to be included in the term. The term is implemented by a wired OR. Noise anded with the value of the term anded with the output of the configuration bit determines whether a vertical wired-OR causes the value of each variable to flip.

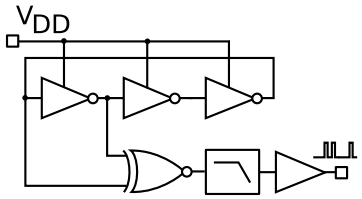

FIGURE 5: Generating random numbers using noise

4.3. Algorithmic description of the hardware solver

The hardware solver can be executed in several modes: fully synchronous, asynchronous, or partially synchronous.

A fully synchronous version of the circuit would use a flip flop to hold the value of each variable, the flip flops would be clocked so that they change states simultaneously, and the clock would run slowly enough to allow the long paths through the logic array to settle down completely. This would cause the circuit to act as a large state machine, and its behaviour would correspond to an algorithm. However, it is costly to propagate a clock through a large circuit, and this approach would use a lot of chip area (reducing the size of problem instance that could be handled) and time (reducing the speed of the search).

A fully asynchronous version of the circuit would allow a variable to change any time a ‘wrong’ signal is received. Different variables would change their values at different times, and the horizontal lines could be calculating results based on variable values that are about to be toggled. The behaviour of the circuit may depend on infinitesimal variations in timing; indeed the results of running the circuit may not be repeatable.

There are also intermediate approaches, where the variables are clocked but the circuit is not completely synchronous.

If the hardware solver were to run in synchronous mode, its behaviour would correspond to a highly parallel randomised algorithm ProbSat:

```
procedure ProbSat;
   input f: array[1..c] of clauses {in CNF}
   output v: array[1..n] of boolean {a  variable assignment that satisfies f}
begin
   v:= random truth assignment;
   while true do
      if all f are true given v then return Success;
      parfor i in [1..n] do
         toggle v[i] with a probability proportional to the number of
                       unsatisfied clauses that contain the variable
end;
```

The hardware solver is an unbounded loop that performs a generate and test strategy. In practice, the circuit is stopped after a fixed number of clock cycles if it has failed to find a solution.

The hardware algorithm differs from WalkSat and GSAT in several respects:

- WalkSat and GSAT toggle a single variable at a time, while the circuit toggles many.
- WalkSat chooses the variable to toggle randomly from a set of clauses where that variable appears, while the circuit bases the decision to toggle a variable on the number of unsatisfied clauses it occurs in. This has something in common with GSAT.
- The hardware solver is highly parallel, speeding up the evaluation of the formula and the selection of variables to toggle.
- The hardware solver can be implemented asynchronously (the pseudo-algorithm shown above is synchronous). An asynchronous circuit may be faster, and it may find a solution more quickly.

5. EXPERIMENTAL RESULTS

We have completed a successful simulation [23] of the hardware SAT solver using FPGA technology (with an Altera Cyclone chip) . An FPGA is a two-dimensional array of programmable components, which are connected by a programmable interconnection network. The circuits used were fully synchronous, but made essential use of randomisation and thus constituted an intermediate point between conventional synchronous circuits, and fully asynchronous circuits. Our circuits are highly parallel. We performed a number of experiments based on a simulation of the circuit using an FPGA chip. As the circuit runs, it may stabilise with a solution for the problem instance, or it may oscillate indefinitely. Thus the circuit corresponds to incomplete software solvers, which may terminate or loop forever.

We developed a prototype compiler that reads an arbitrary instance of 3SAT, and then (in polynomial time) outputs a VHDL specification that describes a circuit specialised to solve that 3SAT instance. The circuit has the structure described above. Altera software tools compile the VHDL specification into the specific machine language programming needed for the Cyclone FPGA. The compilation and control of the FPGA are performed on a host PC.

After the circuit for the problem instance is loaded onto the FPGA, the chip is given a fixed interval of time to run. If it attains a fixed point within this time, the problem instance has been solved, and the exact solution time is measured by an accurate clocked counter on the FPGA. If the circuit does not reach a fixed point, the attempt is abandoned as a failure.

Our experiments compared the performance of the hardware solver with WalkSat, described above. Marked performance gains were observed for the hardware solver in comparison with WalkSat.

According to our preliminary results, the hardware solver gives good results on problem instances that are not too close to the phase change boundary. To achieve this, the solution requires randomisation to determine when variables are changed, and the performance is sensitive to

the toggling probability. The best toggling probability depends slightly on the ratio of clauses to variables; there is not one fixed probability that is always best.

There is wide variation in solution times; sometimes the hardware solver is much faster than software, and sometimes much slower. However, for problem instances that are relatively easy (i.e. which have a solution which is not near the phase boundary) the hardware solver is on average significantly faster, and there are many such cases.

6. CONCLUSION

We have presented a design paradigm that exploits some of the capabilities of physical systems comprising networks of Boolean logic gates in order to solve instances of an NP-complete problem. The feasibility of this approach has been demonstrated by parallel hardware simulation using FPGA technology. However, FPGAs cannot achieve the full performance inherent in our technique, so future research will require the design of suitable programmable array circuits using ASIC (application-specific integrated circuit) technology.

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